PET-5H002 DIGITAL VLSI DESIGN

Module-1

Chapter-1: Introduction

Multiple Choice Questions:

1. VLSI technology uses _____ to form ICs.
a) transistors
b) switches
c) diodes
d) capacitors

2. very large scale integration has
a) ten logic gates
b) fifty logic gates
c) hundred logic gates
d) thousands logic gates

3. The difficulty in achieving high doping concentration leads to
a) error in concentration
b) error in variation
c) error in doping
d) distribution error

4. _____ is used to deal with effect of variation
a) chip level
b) logic level
c) switch level
d) system level

5. As die size shrinks, the complexity of making the photomasks
a) increases
b) decreases
c) remains the same
d) cannot be determined

6. _____ architecture is used to design VLSI
a) system on a device
b) single open circuit
c) system on a chip
d) system on a circuit

7. _____ is used in logic design of VLSI
a) LIFO
b) FIFO
c) FILO
d) None of the above

.

8. Which provides higher integration density?
a) switch transistor logic
b) transistor buffer logic
c) transistor transistor logic
d) circuit level logic

9. Physical and electrical specification is given in
a) architectural design
b) logic design
c) system design
d) functional design

10. As source drain voltage increases, channel depth
a) increases
b) decreases
c) logarithmically increases
d) exponentially increases

11. Inversion layer in enhancement mode consists of excess of
a) positive carriers
b) negative carriers
c) both in equal quantity
d) neutral carriers

12. The VLSI Design methodologies include

a) Full custom and semicustom design
b) FPGA design
c) Y-Chart
d) None

13. The main element of FPGA chip is
a) Gates
b) CLBs
c) CPLD
d) I/O buffers

14. The DRC Check of the digital circuits are implemented with the help of
a) FPGA
b) Standard cell based design
c) Gate array design
d) CAD Tools

15. The high speed circuits are
a) VLSI circuits
b) CMOS circuits
c) Gallium Arsenide (GaAs) circuits
d) PMOS circuits

16. Simple Programmable Logic Devices (SPLDs) are also regarded as _____.
a. Programmable Array Logic (PAL)
b. Generic Array Logic (GAL)
c. Programmable Logic Array (PLA)
d. All of the above

17. In floorplanning, placement and routing are _____ tools.
a. Front end
b. Back end
c. Both a and b
d. None of the above

18. According to Moore's law, the number of transistors that could be manufactured on a chip
a) linearly decreases
b) grows exponentially
c) grows linearly
d) decreases exponentially
19. In logic synthesis, _____ is an EDIF that gives the description of logic cells & their interconnections.
a. Netlist
b. Checklist
c. Shitlist
d. Dualist
20. Which level of system implementation includes the specific function oriented registers, counters & multiplexers?
a. Module level
b. Logical level
c. Physical level
d. All of the above

21. Which among the following is/are taken into account for post-layout simulation?
a. Interconnect delays
b. Propagation delays
c. Logic cells
d. All of the above
22. Physical verification tools in CAD design process includes
a) circuit extractors
b) textual entry
c) graphical entry
d) simulation
23. Behavioral tools of CAD contains
a) graphical entry
b) design check
c) performance check
d) simulation
24. Selection and placement is done using
a) cursor
b) shapes
c) textual
d) graphical
25. Which is used to interpret physical layout in circuit terms?
a) circuit converter
b) layout converter
c) circuit extractor
d) layout extractor

Key Answers:

1(a), 2(d), 3(b), 4(d), 5(a), 6(c), 7(b), 8(c), 9(d),10(b), 11(b), 12(a), 13(b), 14(d), 15(c) ,16(d),17(b),18(b),19(a),20(a),21(d),22(a), 23(d),24(a),25(c)

SUBJECTIVE QUESTIONS

1. Differentiate between Full custom and semi custom design methodologies available in VLSI.

FULL CUSTOM DESIGN	SEMI CUSTOM DESIGN
All mask layers are customized in full custom design	It uses pre-designed logic cell(and gates, OR gate, multiplexers) known as standard cells.
In full custom design, all logic cells, circuits or layouts are designed specifically. Design doesn't use pretested or pre-characterized cells.	Designer used pre-tested or pre-characterized cell.
This approach is considered only when there is no suitable existing	Widely used
Offers high performance lower cost as compared to semi.	More cost. Low performance.
Design time and complexity is more.	Design time and complexity is less
Eg: Microprocessor	Eg. Digital logics

Semi-Custom Design

When manufacturers introduce new products or computers, it is ideal to introduce them with the highest performance in the shortest time. Design of logic networks with the highest performance requires deliberate design of logic networks, design of transistor circuits, layout of these transistor circuits most compactly, and manufacturing of them. Such logic networks are called random-logic gate networks and are realized by full-custom design. In contrast to full-custom design, semi-custom design simplifies design and layout of transistor circuits to save expenses and design time. Depending on how design and layout of transistor circuits are

simplified (e.g., repetition of small transistor sub circuit, or not so compact layout) and even how logic design is simplified, we have variants of semi-custom design.

Full-Custom Design

Full-custom design is logic design to attain the highest performance or smallest size, utilizing the most advanced technology. Designers usually try to improve the economic aspect, that is, performance per cost, at the same time. Full-custom design with the most advanced technology usually takes many years to achieve final products, because new technology must often be explored at the same time. Hence, this is the other extreme to the above quick design in terms of design time. Every design stage is carefully done for the maximum performance, and transistor circuits are deliberately laid out on chips most compactly, spending months by many draft people and engineers.

2. Discuss about Moore's Law.

Ans: In the 1960s, Gordon Moore, then with Fairchild Corporation and later cofounder of Intel, predicted that the number of transistors that can be integrated on a single die would grow exponentially with time. This prediction, later called *Moore's law*, has proven to be amazingly visionary. Its validity is best illustrated with the aid of a set of graphs. Figure 1 plots the integration density of both logic IC's and memory as a function of time. As can be observed, integration complexity doubles approximately every 1 to 2 years. As a result, memory density has increased by more than a thousand fold since 1970.

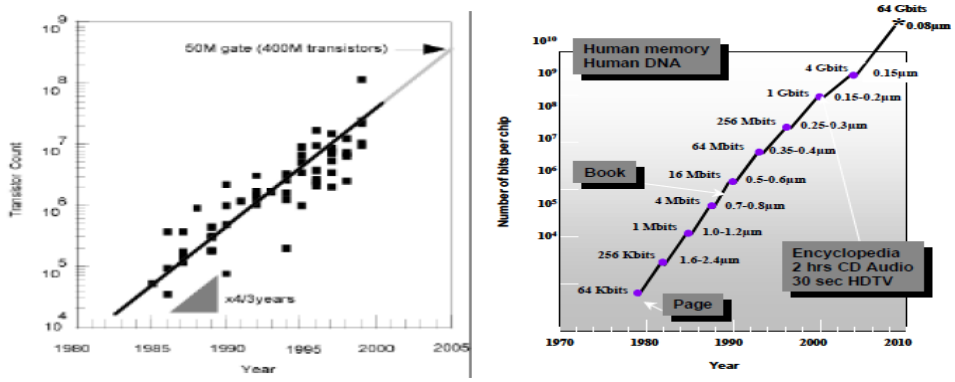
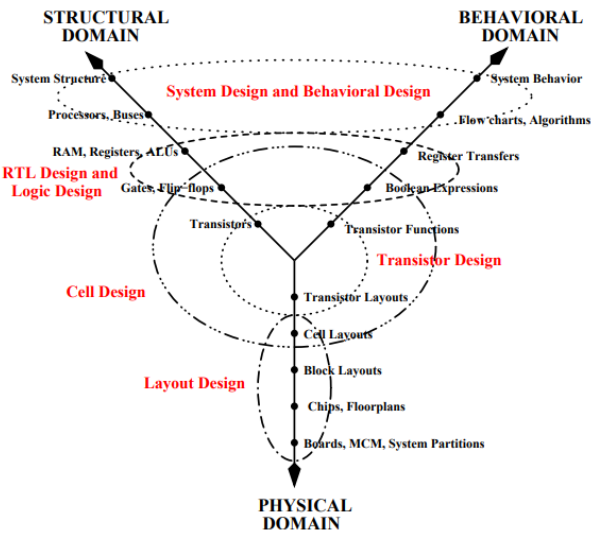


Figure 1: Evolution of integration complexity of logic ICs and memories as a function of time.

3. Describe about the VLSI Design Flow with the help of a Y- chart.

Ans: The figure below shows the Y-Chart designed by D. Gajski and the various levels of abstraction:



The above Y-chart is briefly explained as under:

1. SPECIFICATION: This is the crucial step as it will decide the future of the product. Lots of activity goes on to gather the market requirement. One may take feedback from potential customers on what they are looking for or what the expectations are. Once this done, the specification sheet along with finer technical details are shared to next team.
2. ARCHITECTURE: Now this is the step where main work starts. With the help of specification, design engineers decide the architecture and a layout is created for the IC using EDA tools.
3. RTL CODING: RTL is an acronym for register transfer level. This is where the detailed system specifications is converted into VHDL or Verilog language (Hardware Description Language) showing how data is transferred from register to register. This also goes through functional verification process in next step.
4. RTL VERIFICATION: Register Transfer level is one of the important step which ensures that the design is logically correct without major timing errors. It is very advantageous to perform this step at early stage. A testbench file may be used to verify the design using EDA tools.
5. SYNTHESIS: In this process RTL is transferred to netlist (gate level netlist). This is done with the help of FPGA/CPLD/ASIC hardware tools. These target boards may be accessed using IDE's provided by different vendors.
6. GATE-LEVEL SIMULATION: The verification of gate level simulation of the logic generated is very important. In this step various kinds of checks are included like: functionality check, timing check and physical analysis check.
7. BACK-END: Here the final design after synthesis is given to the IC manufacturer.
8. TAPE-OUT: It is the process under back-end only where the final result of FRONT-END is provided to the manufacturer in form of photomask. Then the manufacturer performs wafer processing, packaging, testing, and delivery of samples to test the physical IC.

9. TO FOUNDRY: once the samples are tested and verified, then the design is sent for mass production.

4. What do you mean by Regularity, Modularity and locality in VLSI?

Ans. **Regularity** means that the hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. A good example of regularity is the design of array structures consisting of identical cells - such as a parallel multiplication array. Regularity can exist at all levels of abstraction: At the transistor level, uniformly sized transistors simplify the design. At the logic level, identical gate structures can be used, etc. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

Modularity in design means that the various functional blocks which make up the larger system must have well-defined functions and interfaces. Modularity allows that each block or module can be designed relatively independently from each other, since there is no ambiguity about the function and the signal interface of these blocks. All of the blocks can be combined with ease at the end of the design process, to form the large system. The concept of modularity enables the parallelization of the design process. It also allows the use of generic modules in various designs - the well-defined functionality and signal interface allow plug-and-play design.

Locality: The concept of locality also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible. This last point is extremely important for avoiding excessive interconnect delays. Time-critical operations should be performed locally, without the need to access distant modules or signals. If necessary, the replication of some logic may solve this problem in large system architectures.

5. Describe the brief architecture of FPGA.

Ans: A typical field programmable gate array (FPGA) chip consists of I/O buffers, an array of configurable logic blocks (CLBs), and programmable interconnect structures. The programming of the interconnects is implemented by programming of RAM cells whose output terminals are connected to the gates of MOS pass transistors. A general architecture of FPGA from XILINX is shown in Fig. 1. A more detailed view showing the locations of switch matrices used for interconnect routing is given in Fig. 1.

A simple CLB (model XC2000 from XILINX) is shown in Fig. 2. It consists of four signal input terminals (A, B, C, D), a clock signal terminal, user-programmable multiplexers, an SR-latch, and a look-up table (LUT). The LUT is a digital memory that stores the truth table of the Boolean function. Thus, it can generate any function of up to four variables or any two functions of three variables. The control terminals of multiplexers are not shown explicitly in Fig. 2.

The CLB is configured such that many different logic functions can be realized by programming its array. More sophisticated CLBs have also been introduced to map complex functions. The typical design flow of an FPGA chip starts with the behavioral description of its functionality, using a hardware description language such as VHDL. The synthesized architecture is then

technology-mapped (or partitioned) into circuits or logic cells. At this stage, the chip design is completely described in terms of available logic cells. Next, the placement and routing step assigns individual logic cells to FPGA sites (CLBs) and determines the routing patterns among the cells in accordance with the netlist. After routing is completed, the on-chip performance of the design can be simulated and verified before downloading the design for programming of the FPGA chip. The programming of the chip remains valid as long as the chip is powered-on, or until new programming is done. In most cases, full utilization of the FPGA chip area is not possible - many cell sites may remain unused.

The largest advantage of FPGA-based design is the very short turn-around time, i.e., the time required from the start of the design process until a functional chip is available. Since no physical manufacturing step is necessary for customizing the FPGA chip, a functional sample can be obtained almost as soon as the design is mapped into a specific technology. The typical price of FPGA chips are usually higher than other realization alternatives (such as gate array or standard cells) of the same design, but for small-volume production of ASIC chips and for fast prototyping, FPGA offers a very valuable option.

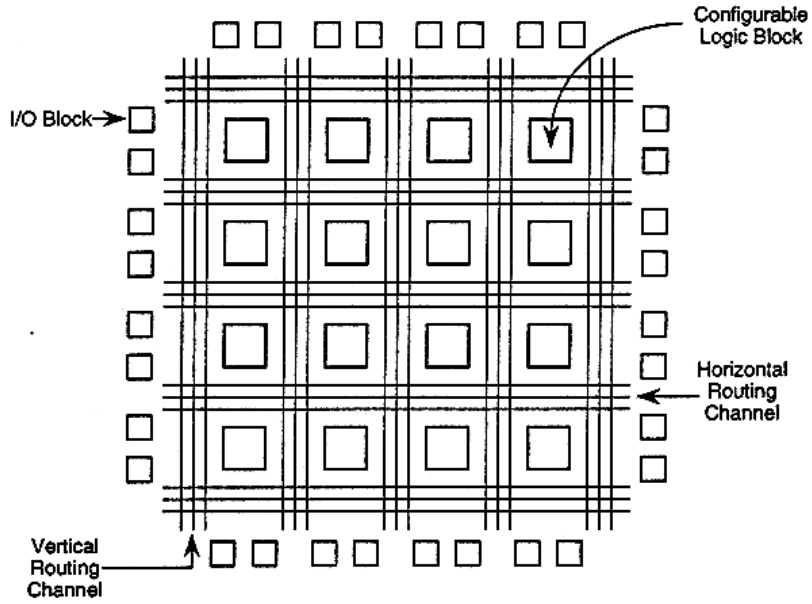


Fig.1. A simple FPGA Chip

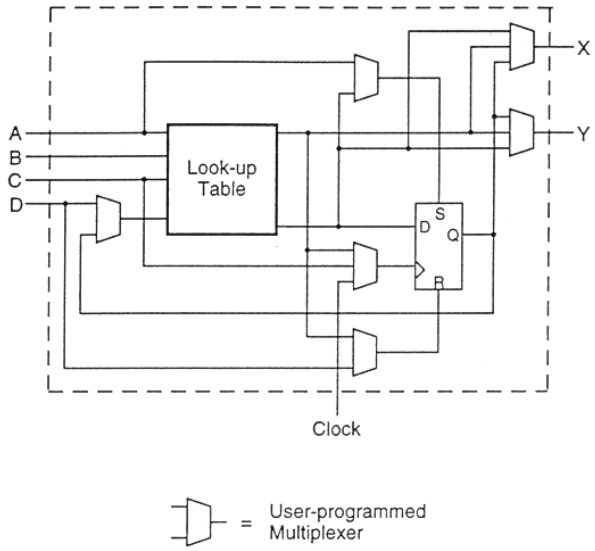


Fig. 2: A CLB of a FPGA chip

6. Compare the full custom design style and semi custom and FPGA design style.

Ans:

Design Styles	Advantages	Disadvantages
Full-Custom	- Compact designs; -Improved electrical characteristics	- Very time consuming; - More error prone;
Semi- Custom	-Well-tested standard cells which can be shared between users; -Good for bottom-up design;	-Can be time consuming to built-up standard cells; -Expensive in the short term but cheaper in long-term costs;
FPGA	-Fast implementation; -Easy updates;	-Can be wasteful of space and pin connections; -Relatively expensive in large volumes;

7. Explain Design Hierarchy with the help of an example.

Ans:

- Based on divide and conquer
- Dividing a module into sub- modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.
- In fig., CMOS four-bit adder into its components.
- The adder can be decomposed progressively into one bit adders, separate carry and sum circuits, and finally, into individual logic gates. At this lower level of the hierarchy, the design of a simple circuit realizing a well-defined Boolean function is much more easier to handle than at the higher levels of the hierarchy.

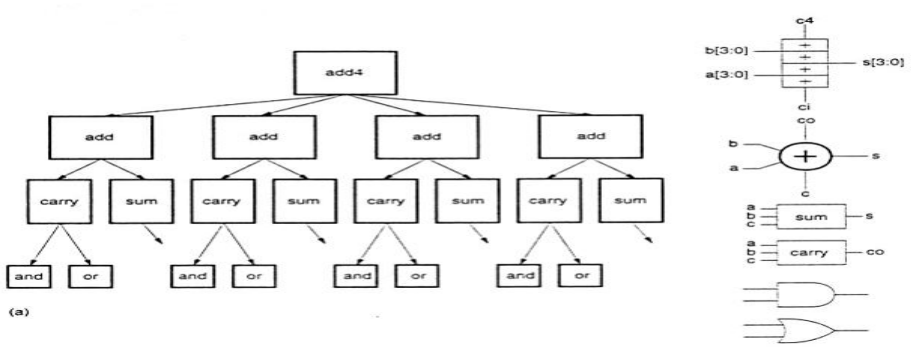


Fig (a) : A 4 bit adder circuit as an example of design hierarchy

8. Explain the scale of integration in the field of IC technology.

Ans:

Scale of Integration:

Small scale integration(SSI) –1960

- The technology was developed by integrating the number of transistors of 1-100 on a single chip. Ex: Gates, flip-flops, op-amps.

Medium scale integration(MSI) –1967

- The technology was developed by integrating the number of transistors of 100- 1000 on a single chip. Ex: Counters, MUX, adders, 4-bit microprocessors.

Large scale integration(LSI) –1972

- The technology was developed by integrating the number of transistors of 1000- 10000 on a single chip. Ex:8-bit microprocessors,ROM,RAM.

Very large scale integration(VLSI) -1978

- The technology was developed by integrating the number of transistors of 10000- 1Million on a single chip. Ex:16-32 bit microprocessors, peripherals, complimentary high MOS.

Ultra large scale integration(ULSI)

- The technology was developed by integrating the number of transistors of 1Million- 10 Millions on a single chip. Ex: special purpose processors.

Giant scale integration(GSI)

- The technology was developed by integrating the number of transistors of above 10 Millions on a single chip. Ex: Embedded system, system on chip.

Fabrication technology has advanced to the point that we can put a complete system on a single chip. Single chip computer can include a CPU, bus, I/O devices and memory. This reduces the manufacturing cost than the equivalent board level system with higher performance and lower power.

9. What is CAD? Discuss the advantages of CAD in VLSI?

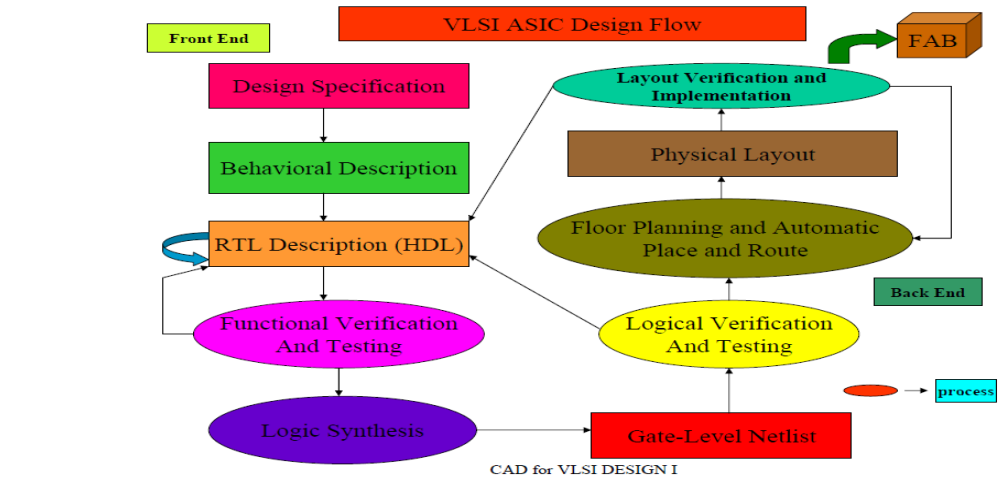
Ans: Computer aided design can be defined as any design that involves the effective use of computers to create, modify or document an engineering design.

Advantages:

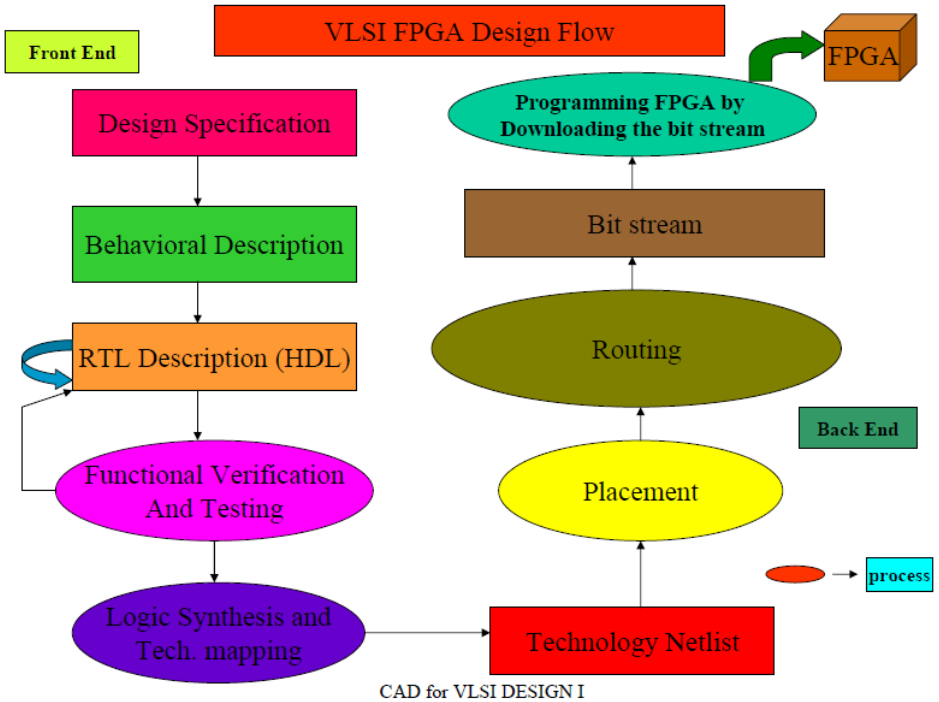
- High productivity and reduced lead time.
- Accuracy in design.
- Better central over the complete project process.
- Modifications in design relatively easy.
- Simulations of the computer generated model can reduce or eliminate prototype testing.
- Effective creation of manufacturing documentation.
- Optimized solution can be received.

10. Explain the steps of CAD Technology.

Ans:



CAD for VLSI DESIGN I



CAD for VLSI DESIGN I

Modern design systems use a variety of CAD tools, including:

1. Design-capture tools – These tools help translate an idea into a high-level design description .
2. Synthesis tools – These tools translate a higher-level description into a lower level one.
3. Verification tools – These tools verify that a lower-level implementation is equivalent to a higher-level one .

Typically, the design process is not completely automated. Instead, the various CAD tools are used at the designer's discretion to facilitate and validate the design tasks. CAD tools need to understand both the language and the primitives that the language refers to

1. Design Capture Tools

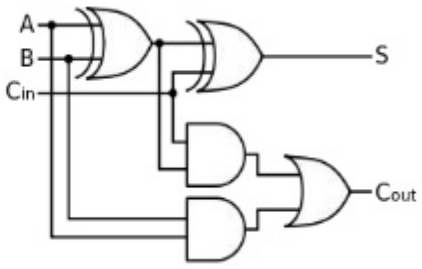
Design-capture tools are the first tools to be used. They provide an interface between what the designer has in mind and the high-level design description. There are two general methods of design capture :

a) Textual

b) Schematic

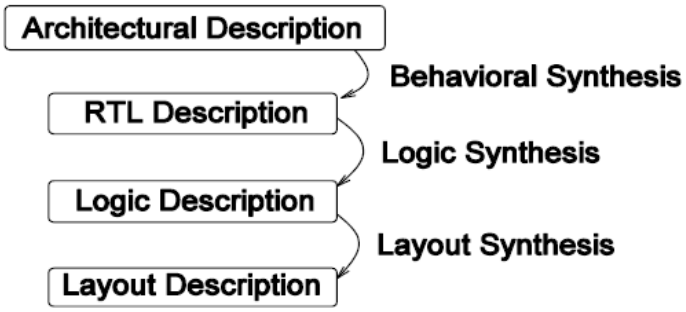
Definition of 1-bit Full adder will be as follow :

```
module FullAdder(A,B,Cin,Cout,S);
 input   A, B, Cin;
 output  Cout, S;
 // Design Body
endmodule
```



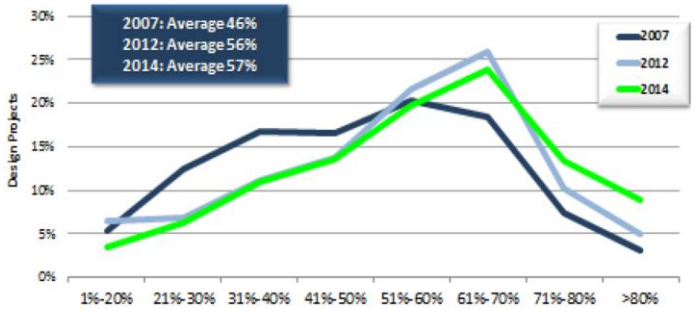
2. Synthesis Tools:

Effectively, these tools transform the design specification from the abstract (high-level) to the concrete (low-level) – For example: given a Boolean function, find a "good" choice and arrangement of logic gates that implement that function. – The solution to this problem is what is called logic synthesis. As the name implies, synthesis tools build the design.



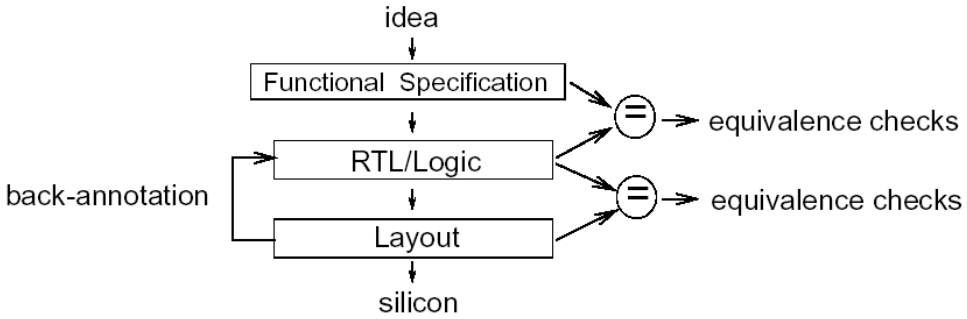
3. Formal Verification

Over 50% of project time spent in verification



It is always important to verify equivalence between different levels of the design.

•Simulation tools
•Timing verification tools
•Formal verification tools

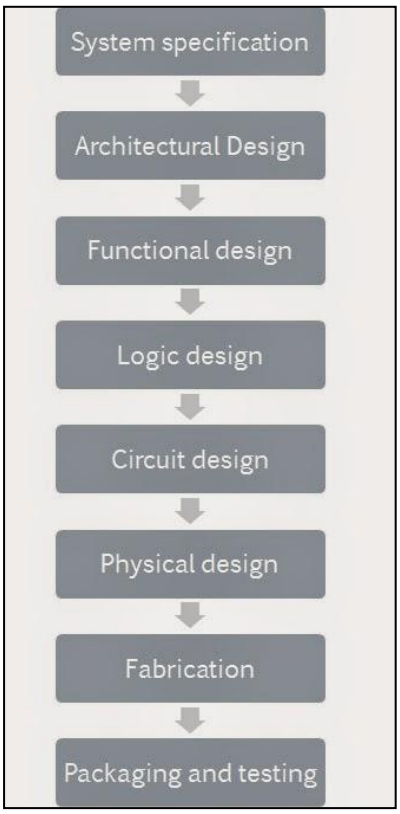


- It aims to directly *prove* the equivalence of two design representations.
- For instance, *graph isomorphism* is applied to check that a transistor netlist is identical to an extracted netlist.
- These methods are mature and well developed
- The main challenge is scalability
- Many commercial tools available
- SoC verification is still a challenge
- Simulators are probably the most often used design tools.
- A simulator uses mathematical models to represent the behavior of circuit components.
- Given specific input signals, the simulator solves for the signals inside the circuit.
- Simulators come in a wide variety depending on the level of accuracy and the simulation speed desired:
- circuit simulation
- switch-level simulation, logic simulation, functional simulation.

11. Draw the flow chart of VLSI design methodology and explain briefly.

Ans:

VLSI Design methodology



VLSI design Flow

The VLSI design cycle starts with a formal specification of a VLSI chip, follows a series of steps, and eventually produces a packaged chip. A typical design cycle may be represented by the flow chart shown in Figure. Our emphasis is on the physical design step of the VLSI design cycle. However, to gain a global perspective, we briefly outline all the steps of the VLSI design cycle.

1.System Specification:

- The first step of any design process is to lay down the specifications of the system. System specification is a high level representation of the system. The factors to be considered in this process include: performance, functionality, and physical dimensions (size of the die (chip)). The fabrication technology and design techniques are also considered.

- The specification of a system is a compromise between market requirements, technology and economical viability. The end results are specifications for the size, speed, power, and functionality of the VLSI system.

2. Architectural Design:

- The basic architecture of the system is designed in this step. This includes, such decisions as RISC (Reduced Instruction Set Computer) versus CISC (Complex Instruction Set Computer), number of ALUs, Floating Point units, number and structure of pipelines, and size of caches among others.
- The outcome of architectural design is a Micro-Architectural Specification (MAS). While MAS is a textual (English like) description, architects can accurately predict the performance, power and die size of the design based on such a description.

3. Behavioral or Functional Design:

- In this step, main functional units of the system are identified. This also identifies the interconnect requirements between the units. The area, power, and other parameters of each unit are estimated.
- The behavioral aspects of the system are considered without implementation specific information. For example, it may specify that a multiplication is required, but exactly in which mode such multiplication may be executed is not specified. We may use a variety of multiplication hardware depending on the speed and word size requirements. The key idea is to specify behavior, in terms of input, output and timing of each unit, without specifying its internal structure.
- The outcome of functional design is usually a timing diagram or other relationships between units. This information leads to improvement of the overall design process and reduction of the complexity of subsequent phases. Functional or behavioral design provides quick emulation of the system and allows fast debugging of the full system. Behavioral design is largely a manual step with little or no automation help available.

4. Logic Design:

- In this step the control flow, word widths, register allocation, arithmetic operations, and logic operations of the design that represent the functional design are derived and tested.
- This description is called Register Transfer Level (RTL) description. RTL is expressed in a Hardware Description Language (HDL), such as VHDL or Verilog. This description can be used in simulation and verification. This description consists of Boolean expressions and timing information. The Boolean expressions are minimized to achieve the smallest logic design which conforms to the functional design. This logic design of the system is simulated and tested to verify its correctness. In some special cases, logic design can be automated using *high level synthesis* tools. These tools produce a RTL description from a behavioral description of the design.

5. Circuit Design:

- The purpose of circuit design is to develop a circuit representation based on the logic design. The Boolean expressions are converted into a circuit representation by taking into consideration the speed and power requirements of the original design. *Circuit Simulation* is used to verify the correctness and timing of each component.
- The circuit design is usually expressed in a detailed circuit diagram. This diagram shows the circuit elements (cells, macros, gates, transistors) and interconnection between these elements. This representation is also called a *netlist.* Tools used to manually enter such description are called *schematic capture tools.* In many cases, a netlist can be created automatically from logic (RTL) description by using *logic synthesis* tools.

6. Physical Design:

- In this step the circuit representation (or netlist) is converted into a geometric representation. As stated earlier, this geometric representation of a circuit is called a *layout.* Layout is created by converting each logic component (cells, macros, gates, transistors) into a geometric representation (specific shapes in multiple layers), which perform the intended logic function of the corresponding component. Connections between different components are also expressed as geometric patterns typically lines in multiple layers.
- The exact details of the layout also depend on design rules, which are guidelines based on the limitations of the fabrication process and the electrical properties of the fabrication materials. Physical design is a very complex process and therefore it is usually broken down into various sub-steps. Various verification and validation checks are performed on the layout during physical design.
- In many cases, physical design can be completely or partially automated and layout can be generated directly from netlist by *Layout Synthesis* tools. Layout synthesis tools, while fast, do have an area and performance penalty, which limit their use to some designs. Manual layout, while slow and manually intensive, does have better area and performance as compared to synthesized layout. However this advantage may dissipate as larger and larger designs may undermine human capability to comprehend and obtain globally optimized solutions.

7. Fabrication:

- After layout and verification, the design is ready for fabrication. Since layout data is typically sent to fabrication on a tape, the event of release of data is called *Tape Out.* Layout data is converted (or fractured) into photo-lithographic masks, one for each layer. Masks identify spaces on the wafer, where certain materials need to be deposited, diffused or even removed. Silicon crystals are grown and sliced to produce wafers. Extremely small dimensions of VLSI devices require that the wafers be polished to near

perfection. The fabrication process consists of several steps involving deposition, and diffusion of various materials on the wafer. During each step one mask is used. Several dozen masks may be used to complete the fabrication process.

- A large wafer is 20 cm (8 inch) in diameter and can be used to produce hundreds of chips, depending of the size of the chip. Before the chip is mass produced, a prototype is made and tested. Industry is rapidly moving towards a 30 cm (12 inch) wafer allowing even more chips per wafer leading to lower cost per chip.

8. Packaging, Testing and Debugging:

- Finally, the wafer is fabricated and diced into individual chips in a fabrication facility. Each chip is then packaged and tested to ensure that it meets all the design specifications and that it functions properly. Chips used in Printed Circuit Boards (PCBs) are packaged in Dual In-line Package (DIP), Pin Grid Array (PGA), Ball Grid Array (BGA), and Quad Flat Package (QFP). Chips used in Multi-Chip Modules (MCM) are not packaged, since MCMs use bare or naked chips.

Chapter-2: Fabrication of MOSFETs:

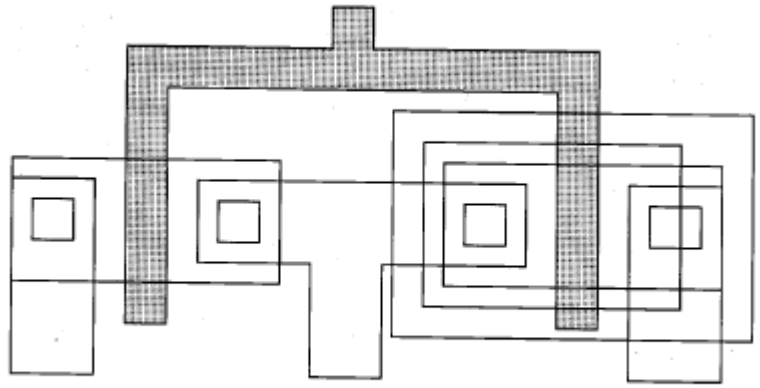
MULTIPLE CHOICE QUESTIONS:

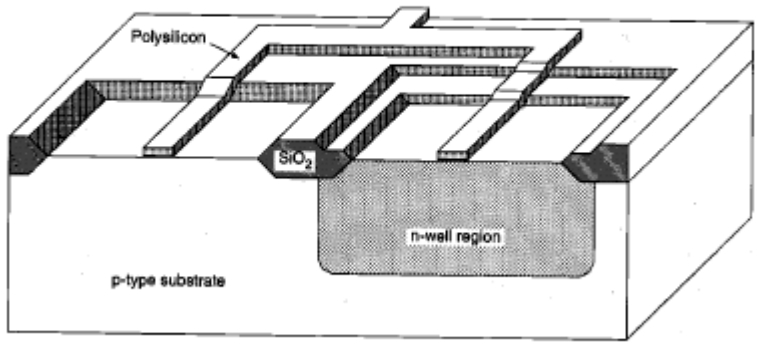
1. P-well is created on
   a) p substrate
   b) n substrate
   c) p & n substrate
   d) none of the mentioned
2. Photoresist layer is formed using
   a) high sensitive polymer
   b) light sensitive polymer
   c) polysilicon
   d) silicon di oxide
3. In CMOS fabrication, the photoresist layer is exposed to
   a) visible light
   b) ultraviolet light
   c) infra red light
   d) fluorescent
4. Few parts of photoresist layer is removed by using
   a) acidic solution
   b) neutral solution
   c) pure water
   d) diluted water
5. Oxidation process is carried out using
   a) hydrogen
   b) low purity oxygen
   c) sulphur
   d) nitrogen
6. P-well doping concentration and depth will affect the
   a) threshold voltage
   b) Vss
   c) Vdd
   d) Vgs
7. Which type of CMOS circuits are good and better?
   a) p well
   b) n well
   c) all of the mentioned
   d) none of the mentioned
8. N-well is formed by
   a) decomposition
   b) diffusion
   c) dispersion
   d) filtering
9. _____ is sputtered on the whole wafer
   a) silicon
   b) calcium
   c) potassium
   d) aluminium
10. CMOS technology is used in developing
   a) microprocessors
   b) microcontrollers
   c) digital logic circuits
   d) all of the mentioned

11. CMOS has
    a) high noise margin
    b) high packing density
    c) high power dissipation
    d) high complexity
12. In CMOS fabrication, nMOS and pMOS are integrated in same substrate.
    a) true
    b) false
13. In nMOS fabrication, etching is done using
    a) plasma
    b) hydrochloric acid
    c) sulphuric acid
    d) sodium chloride
14. In nMOS device, gate material could be
    a) silicon
    b) polysilicon
    c) boron
    d) phosphorus
15. The commonly used bulk substrate in nMOS fabrication is
    a) silicon crystal
    b) silicon-on-sapphire
    c) phosphorus
    d) silicon-di-oxide
16. Heavily doped polysilicon is deposited using
    a) chemical vapour decomposition
    b) chemical vapour deposition
    c) chemical deposition
    d) dry deposition
17. In diffusion process, _____ impurity is desired
    a) n type
    b) p type
    c) none
18. Interconnection pattern is made on
    a) polysilicon layer
    b) silicon-di-oxide layer
    c) metal layer
    d) diffusion layer
19. _____ is used to suppress unwanted conduction
    a) phosporus
    b) boron
    c) silicon
    d) oxygen
20. Which is used for the interconnection?
    a) boron
    b) oxygen
    c) aluminium
    d) silicon

21. nMOS fabrication process is carried out in
    a) thin wafer of a single crystal
    b) thin wafer of multiple crystals
    c) thick wafer of a single crystal
    d) thick wafer of multiple crystals
22. _____ impurities are added to the wafer of the crystal
    a) n impurities
    b) p impurities
    c) silicon
    d) crystal
23. What kind of substrate is provided above the barrier to dopants?
    a) insulating
    b) conducting
    c) silicon
    d) semi conducting
24. Chemical Mechanical Polisihing is used to:
    a) Remove silicon oxide
    b) Remove silicon nitride and pad oxide
    c) Remove polysilicon gate layer
    d) Reduce the size of the layout
25. Gate oxide layer consists of:
    a) SiO2 layer, overlaid with a few layers of an oxynitride oxide
    b) Only SiO2 Layer
    c) SiO2 layer with Polysilicon Layer
    d) SiO2 layer and stack of epitaxial layers of Polysilicon
26. What is Piranha Solution
    a) It is a 3:1 to 5:1 mix of nitric acid and hydrogen peroxide that is used to develop the oxide layer on silicon substrate
    b) It is a 3:1 to 5:1 mix of sulphuric acid and hydrofluoric acid that is used to clean silicon wafers removing organic and metal contaminants or photo resist after metal patterning
    c) It is a 3:1 to 5:1 mix of sulphuric acid and hydrogen peroxide that is used to grow the oxide layer on the silicon
    d) It is a 3:1 to 5:1 mix of sulphuric acid and hydrogen peroxide that is used to clean wafers of organic and metal contaminants or photo resist after metal patterning.

27. The process involved in growing the shaded region is:





a) Chemical vapor deposition (CVD)
b) Sputtering and patterned by etching
c) Chemical vapor deposition (CVD) and patterned by HF acid etching
d) Chemical vapor deposition (CVD) and patterned by dry (plasma) etching

28. The process by which Aluminium is grown over the entire wafer , also filling the contact cuts is:
a) Sputtering
b) Chemical vapour deposition
c) Epitaxial growth
d) Ion Implantation

29. To grow the polysilicon gate layer, the chemical used for chemical vapour deposition is:
a) Silicon Nitride(Si4N3)
b) Silane gas(SiH4)
c) Silicon oxide
d) None of the mentioned

30. Lithography is:
a) Process used to transfer a pattern to a layer on the chip
b) Process used to develop an oxidation layer on the chip
c) Process used to develop a metal layer on the chip
d) Process used to produce the chip

31. Positive photo resists are used more than negative photo resists because:
    a) Negative photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the positive photo resists
    b) Positive photo resists are more sensitive to light, but their photo lithographic resolution is not as high as that of the negative photo resists
    c) Negative photo resists are less sensitive to light
    d) Positive photo resists are less sensitive to light
32. The _____ is used to reduce the resistivity of poly silicon:
    a) Photo resist
    b) Etching
    c) Doping impurities
    d) None of the mentioned
33. An Antifuse programming technology is predominantly associated with _____.
    a. SPLDs
    b. FPGAs
    c. CPLDs
    d. All of the above
34. Higher dose of boron implemented into base collector region. This causes contact resistance & extrinsic base region resistance
    a) Decreased
    b) Increased
    c) not effected
    d) Inversed
35. Channel stop regions implemented in silicon to increase
    a) Isolation
    b) Resistance
    c) Capacitance
    d) conduction
36. Decomposing of BJT in CMOS Technique results ------- latch up
    a) Prevention
    b) Formation
    c) PNPN structure function
    d) Formation of BJT
37. Trench isolation effectively ---------- bipolar transistors
    a) Decouples
    b) Couples
    c) Forms
    d) Lower resistance
38. Purpose of Pad oxide is
    a) Improve adhesiveness
    b) Decrease adhesiveness
    c) Coupling
    d) De-coupling
39. Self aligned structure results
    a) Decrease the overlap capacitance
    b) Increase the overlap capacitance
    c) Increase Capacitance & Resistance
    d) Decrease Capacitance & Resistance
40. Hot electron effect cause
    a) Degradation of gate material
    b) Increase the life of gate
    c) Decrease Capacitance

d) Decrease inductance

41. Boron used to adjust the
    a) Threshold voltage
    b) Current
    c) Power
    d) Inductance
42. Which MOS transistor passes strong logic '1'
    a) pMOS
    b) nMOS
    c) (a) & (b)
    d) None
43. Pinch off occurs in ---------- region
    a) Non saturation
    b) Saturation
    c) cutoff
    d) linear
44. The drain current flow in ideally independent of drain –source voltage when the channel is ---------- ---
    a) strongly depleted
    b) weakly depleted
    c) strongly inverted
    d) weakly inverted
45. ---------- process is used to transfer the layout pattern from masks to wafer.
    a) Diffusion
    b) Isolation
    c) photolithography
    d) metallization
46. The transistor threshold voltage, V_T is ---------- for P type transistor.
    a) positive
    b) negative
    c) zero
    d) Infinity
47. The present feature size of a transistor is ----------
    a) 1 μm
    b) 0.75 μm
    c) 0.13 μm
    d) 0.5 μm
48. Pick out the advantage of IC
    a) Smaller physical size
    b) Low power consumption
    c) Reduced cost
    d) All
49. In the MOSFET, as width of channel increases Id
    a) Increases
    b) decreases
    c) Constant
    d) none
50. Latch – up is caused by
    a) Parasitic R
    b) Parasitic BJT's
    c) (a) & (b)
    d) Parasitic C
51. Pick up latch-up resistant CMOS process

a) n well
b) p well
c) silicon on Insulator
d) all

52. Cascaded inverters are used to drive large _____ loads
a) Capacitive
b) resistive
c) inductive
d) all

53. In which process (CMOS) pFETs are embedded in n well
a) p well
b) n well
c) SOI
d) all

54. In the Pseudo-nMOS logic ---------- transistor is used as pull-up resistor
a)pMOS
b) nMOS
c) Bipolar
d) Unijunction

55. Latch structure is used in ---------- Logic
a)Pseudo-nMOS
b) DCVS
c) Domino
d) all

56. Routing channel is spacing between
a)cell rows
b) cells
c) wires
d) None

57. Feed throughs are used during
a)Placement
b) Routing
c) Floor planning
d) Synthesis

58. For n-type transistor threshold voltage is _____
a) Positive
b) negative
c) zero
d) none

59. In the twin tub process _____ wafer is used
a) p-doped
b) n-doped
c) undoped
d) none

60. nMOS Transistor is fabricated on
a) n-type substrate
b) p-type substrate
c) insulating substrate
d) conducting substrate

61. Stick diagrams are those which convey layer information through
a) thickness
b) color

c) shapes
d) layers

62. Implant is represented using
a) black, dark line
b) black, dotted line
c) yellow, dark line
d) yellow, dotted line

63. n and p transistors are separated by using
a) differentiation line
b) separation line
c) demarcation line
d) black line

64. Which color is used for n-diffusion?
a) red
b) blue
c) green
d) yellow

Answer key: 1(b), 2(b),3(b),4(a),5(a),6(a),7(b),8(b),9(d),10(d),11(b), 12(a), 13(a),14(b), 15(a) , 16(b), 17(a), 18(c), 19(b), 20(c), 21(a), 22(b), 23(a),24(b), 25(a), 26(d), 27(d), 28(a),29(b), 30(a), 31(a), 32(c), 33(b),34(b), 35(a),36(d),37(b), 38(b), 39(c),40(a), 41(a), 42(a), 43(b), 44(a), 45(c), 46(b),47(c), 48(d) , 49(b),50(b), 51(a), 52(a), 53(b), 54(a), 55(b), 56(c), 57(c),58(a),59(c), 60(b), 61(b), 62(d), 63(c), 64(c)

Subjective type questions:

1.What are the basic processes involved in fabricating ICs ?

Ans: 1.Silicon wafer (substrate) preparation
2.Epitaxial growth
3.Oxidation
4.Photolithography
5.Diffusion
6.Ion implantation
7.Isolation technique
8.Metallization
9.Assembly processing & packaging

2. List out the steps used in the preparation of Si – wafers.

Ans: 1.Crystal growth &doping
2.Ingot trimming & grinding
3.Ingot slicing
4.Wafer policing & etching
5.Wafer cleaning

3. Explain the process of oxidation.

Ans:

The silicon wafers are stacked up in a quartz crystal & then inserted into quartz furnace tube. The Si wafers are raised to a high temperature in the range of 950 to 1150°C & at the same time, exposed to a gas containing O_2 or H_2O or both. The chemical action is

$Si + 2H_2O$ -----> $SiO_2 + 2H_2$

4. What is lithography? What are the different types of lithography? What is optical lithography?

Ans:

Lithography is a process by which the pattern appearing on the mask is transferred to the wafer. It involves two steps: the first step requires applying a few drops of photoresist to the surface of the wafer & the second step is spinning the surface to get an even coating of the photoresist across the surface of the wafer.

The different types of lithography are :

1.Photolithography

2.Electron beam lithography

3.X ray beam lithography

4.Ion beam lithography

Optical lithography:

Optical lithography comprises the formation images with visible or UV radiation in a photoresist using contact, proximity or projection printing.

5.Distinguish between dry etching & wet etching.

Dry etching

1.Gaseous mixture is used as the chemical reagent.

2.Smaller line openings(1μm) are possible with dry etching

3.It produces straight walled etching process.

Wet etching

Chemical reagents used are in the liquid form.

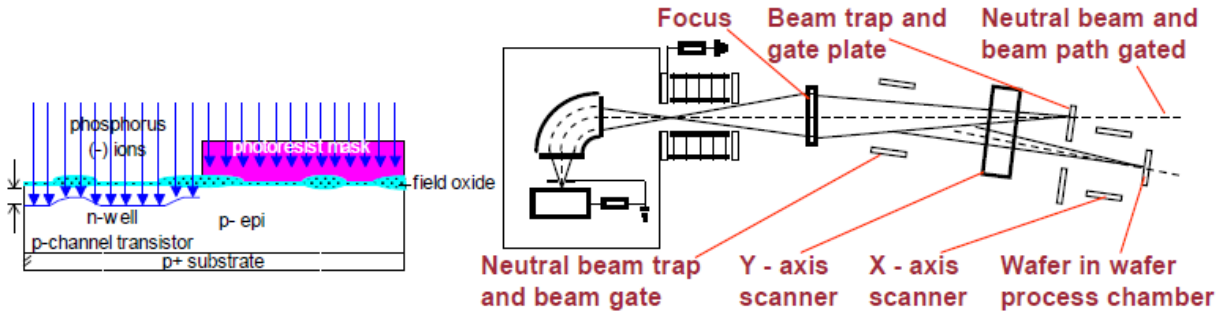
Line opening are larger.(> 1μm)

It produces patterns with undercutting.

6. Define diffusion.

The process of introducing impurities into selected regions of a silicon wafer is called diffusion. The rate at which various impurities diffuse into the silicon will be of the order of 1μm/hr at the temperature range of 900◦C to 1100◦C .The impurity atoms have the tendency to move from regions of higher concentrations to lower concentrations.

7. **What is ion implantation? What are the advantages of ion implantation technique?**



Advantages:

1. It is performed at low temperature. Therefore, previously diffused regions have a lesser tendency for lateral spreading.

2. In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation process, accelerating potential & beam content are dielectrically controlled from outside.

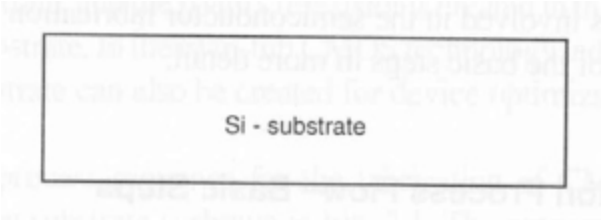
8. Explain the fabrication steps involved in nMOS fabrication .

Ans:

The fabrication steps are as follows:

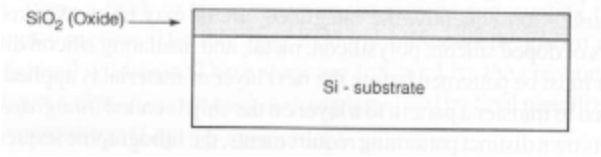
Step1:

Processing is carried on single crystal silicon of high purity on which required P impurities are introduced as crystal is grown. Such wafers are about 75 to 150 mm in diameter and 0.4 mm thick and they are doped with say boron to impurity concentration of 10 to power 15/cm3 to 10 to the power 16 /cm3.



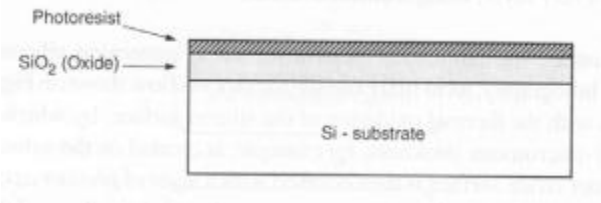
Step 2 :

A layer of silicon di oxide (SiO2) typically 1 micrometer thick is grown all over the surface of the wafer to protect the surface, acts as a barrier to the dopant during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.



Step 3:

The surface is now covered with the photo resist which is deposited onto the wafer and spun to an even distribution of the required thickness.

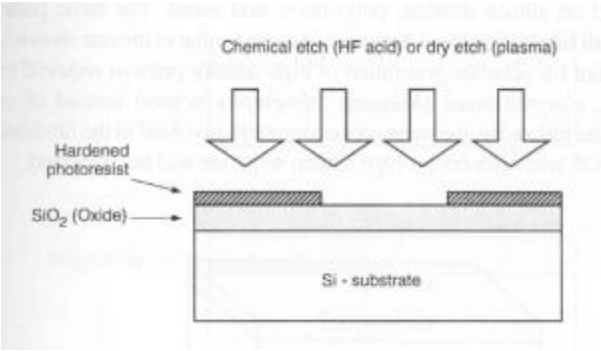


Step 4:

The photo resist layer is then exposed to ultraviolet light through masking which defines those regions into which diffusion is to take place together with transistor channels. Assume, for example , that those areas exposed to uv radiations are polymerized (hardened), but that the areas required for diffusion are shielded by the mask and remain unaffected.

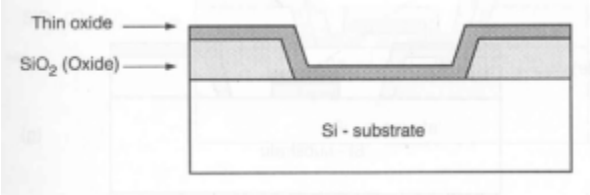
Step 5:

These areas are subsequently readily etched away together with the underlying silicon di oxide so that the wafer surface is exposed in the window defined by the mask.



Step 6:

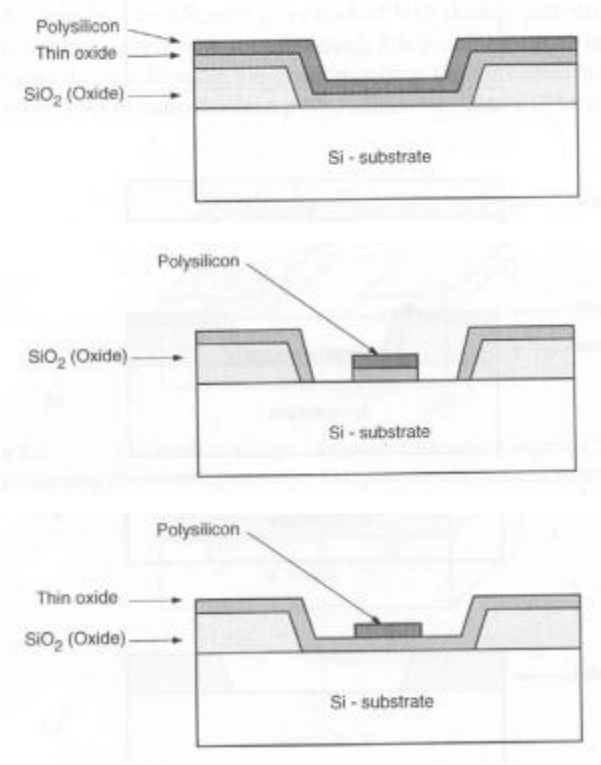
The remaining photo resist is removed and a thin layer of SiO2 (0.1 micro m typical) is grown over the entire chip surface and then poly silicon is deposited on the top of this to form the gate structure. The polysilicon layer consists of heavily doped polysilicon deposited by chemical vapour deposition (CVD). In the fabrication of fine pattern devices, precise control of thickness, impurity concentration, and resistivity is necessary



Step 7:

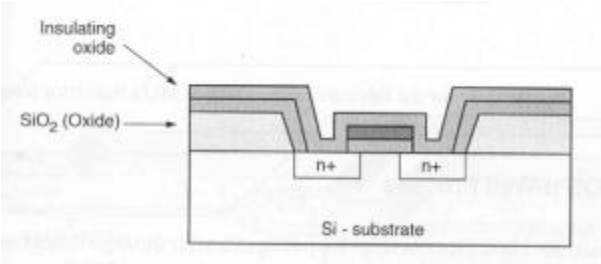
Further photo resist coating and masking allows the poly silicon to be patterned and then the thin oxide is removed to expose areas into which n-type impurities are to be diffused to form the source and drain. Diffusion is achieved by heating the wafer to a high temperature and passing a gas containing the desired n-type impurity.

Note: The poly silicon with underlying thin oxide and the thick oxide acts as mask during diffusion the process is self aligning.



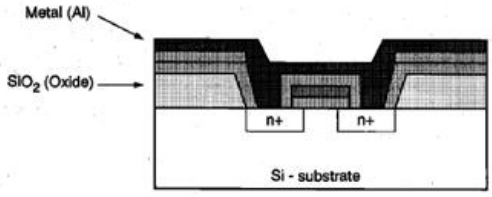
Step 8:

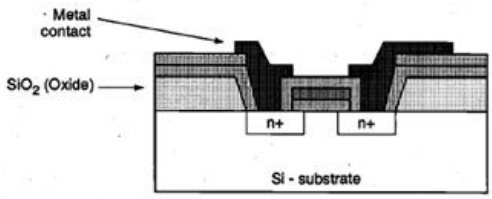
Thick oxide (SiO2) is grown over all again and is then masked with photo resist and etched to expose selected areas of the poly silicon gate and the drain and source areas where connections are to be made. (contacts cut)



Step 9:

The whole chip then has metal (aluminium) deposited over its surface to a thickness typically of 1 micro m. This metal layer is then masked and etched to form the required interconnection pattern.



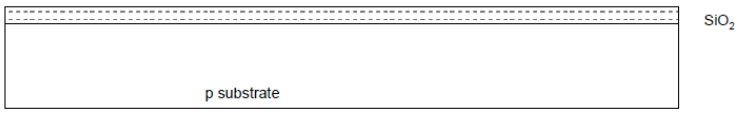


9. Explain the fabrication steps involved in CMOS n well process

Ans:

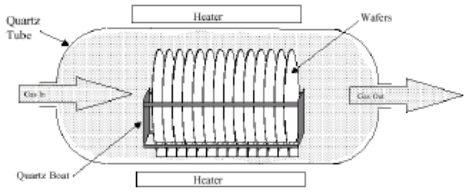
Step 1: First we choose a substrate as a base for fabrication. For N- well, a P-type silicon substrate is selected.

Step 2 – Oxidation: The selective diffusion of n-type impurities is accomplished using SiO2 as a barrier which protects portions of the wafer against contamination of the substrate. SiO_2 is laid out by oxidation process done exposing the substrate to high-quality oxygen and hydrogen in an oxidation chamber at approximately 1000^0c.



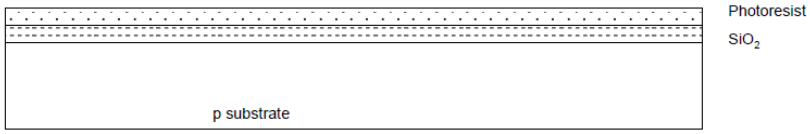
- Heat wafers in an atmosphere containing an oxidant, usually O_2, steam, or N_2O.

$$Si + O_2 \rightarrow SiO_2$$
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$
$$Si + 2N_2O \rightarrow SiO_2 + 2N_2$$

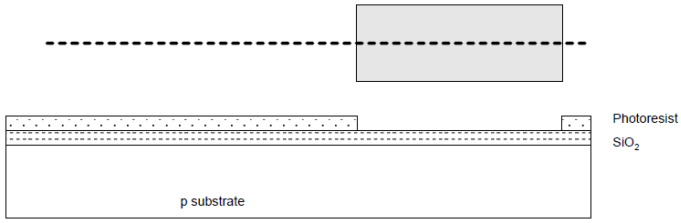


Step 3 – Growing of Photoresist: At this stage to permit the selective etching, the SiO2 layer is subjected to the photolithography process. In this process, the wafer is coated with a uniform film of a photosensitive emulsion.

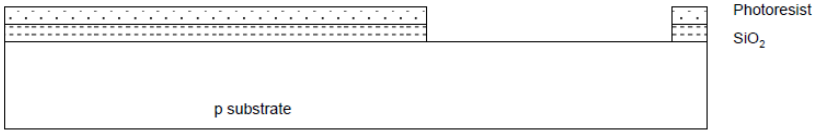
- Photoresist is a light-sensitive organic polymer.
- **Positive Photoresist:** Softens where exposed to light.
- **Negative Photoresist**: Harden where exposed to light, Not used in practice generally.



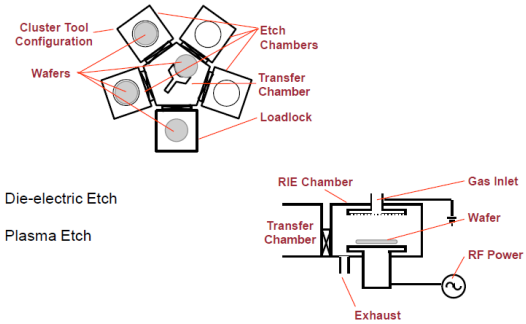
Step 4 – Masking: This step is the continuation of the photolithography process. In this step, a desired pattern of openness is made using a stencil. This stencil is used as a mask over the photoresist. The substrate is now exposed to **UV rays** the photoresist present under the exposed regions of mask gets polymerized.



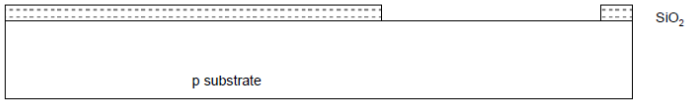
Step 5 – Removal of Unexposed Photoresist: The mask is removed and the unexposed region of photoresist is dissolved by developing wafer using a chemical such as Trichloroethylene.



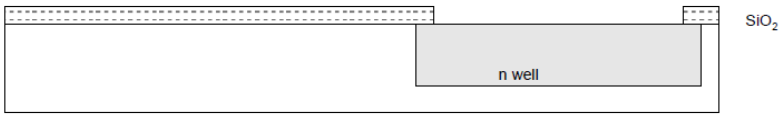
Step 6 – Etching: The wafer is immersed in an etching solution of hydrofluoric acid, which removes the oxide from the areas through which dopants are to be diffused.



Step 7 – Removal of Whole Photoresist Layer: During the **etching process**, those portions of SiO2 which are protected by the photoresist layer are not affected. The photoresist mask is now stripped off with a chemical solvent (hot H2SO4).

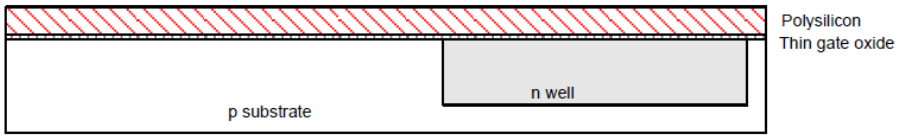


Step 8 – Formation of N-well: The n-type impurities are diffused into the p-type substrate through the exposed region thus forming an N- well.



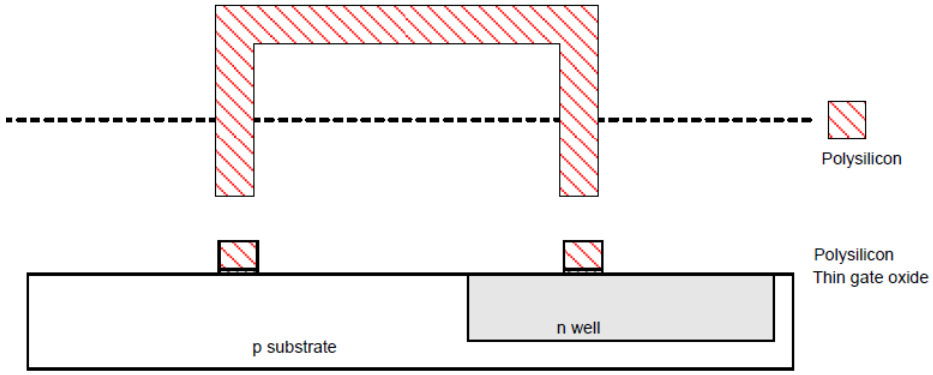
Step 9 – Removal of SiO2: The layer of SiO2 is now removed by using hydrofluoric acid.

Step 10 – Deposition of Polysilicon: The misalignment of the gate of a **CMOS transistor** would lead to the unwanted capacitance which could harm circuit. So to prevent this "Self-aligned gate process" is preferred where gate regions are formed before the formation of source and drain using ion implantation.

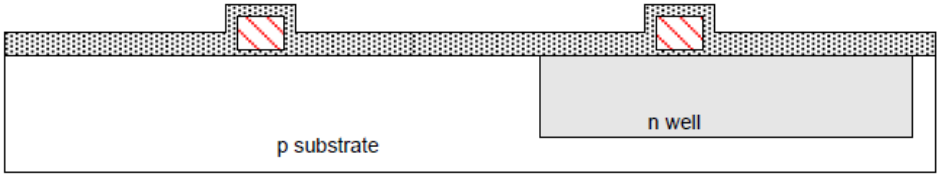


Polysilicon is used for formation of the gate because it can withstand the high temperature greater than 8000^0c when a wafer is subjected to annealing methods for formation of source and drain. Polysilicon is deposited by using **Chemical Deposition Process** over a thin layer of gate oxide. This thin gate oxide under the Polysilicon layer prevents further doping under the gate region.

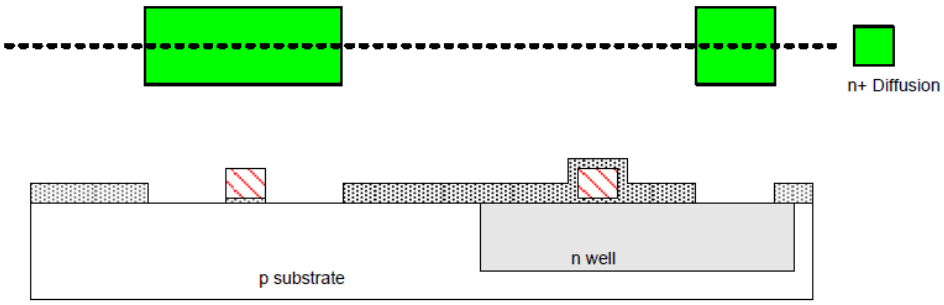
Step 11 – Formation of Gate Region: Except the two regions required for formation of the gate for **NMOS and PMOS transistors** the remaining portion of Polysilicon is stripped off.



Step 12 – Oxidation Process: An oxidation layer is deposited over the wafer which acts as a shield for further **diffusion and metallization processes**.

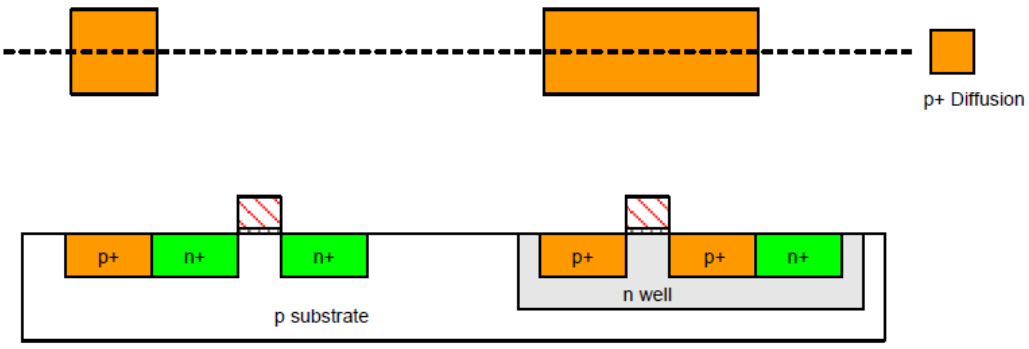


Step 13 – Masking and Diffusion: For making regions for diffusion of n-type impurities using masking process small gaps are made.

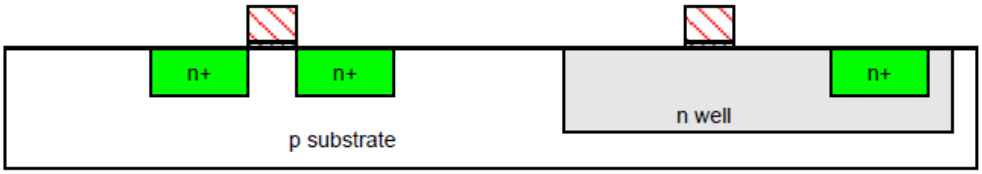


Using diffusion process three n+ regions are developed for the formation of terminals of NMOS.

Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact.



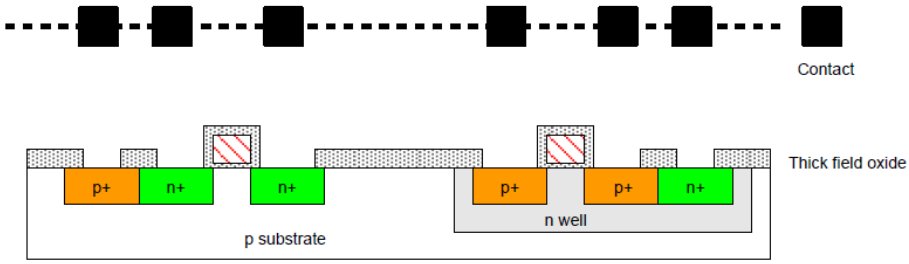
Step 14 – Removal of Oxide: The oxide layer is stripped off.



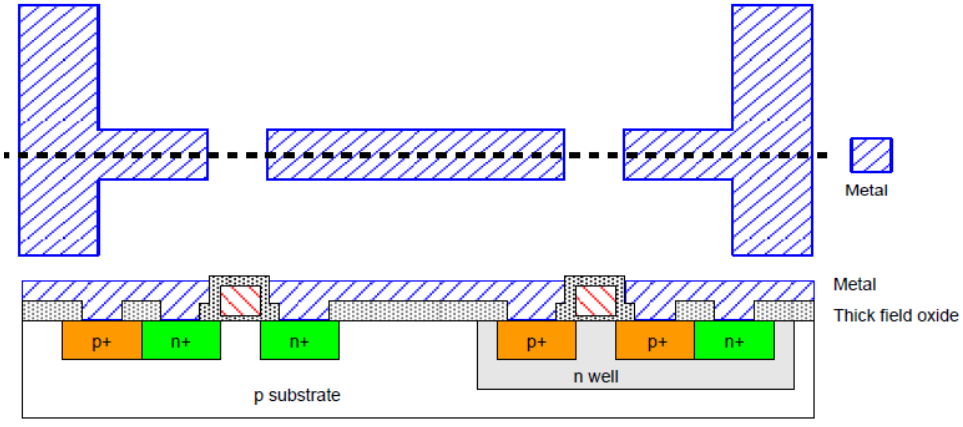
Step 15 – P-type Diffusion: Similar to the n-type diffusion for forming the terminals of PMOS p-type diffusion are carried out.

Step 16 – Laying of Thick Field oxide: Before forming the metal terminals a thick field oxide is laid out to form a protective layer for the regions of the wafer where no terminals are required.

Step 17 – Metallization: This step is used for the formation of metal terminals which can provide interconnections. Aluminum is spread on the whole wafer.



Step 18 – Removal of Excess Metal: The excess metal is removed from the wafer.



10. What is Device isolation technique? Explain the LOCOS Process.

Ans.

The MOS transistors that comprise an integrated circuit must be electrically isolated from each other during fabrication. Isolation is required to prevent unwanted conduction paths between the devices, to avoid creation of

inversion layers outside the channel regions of transistors, and to reduce leakage currents. To achieve a sufficient level of electrical isolation between neighboring transistors on a chip surface, the devices are typically created in dedicated regions called active areas, where each active area is surrounded by a relatively thick oxide barrier called the field oxide.

LOCOS Process:

The local oxidation of silicon (LOCOS) technique is based on the principle of selectively *growing* the field oxide in certain regions, instead of selectively etching away the active areas after oxide growth. Selective oxide growth is achieved by shielding the active areas with silicon nitride (Si3N4) during oxidation, which effectively inhibits oxide growth. The basic steps of the LOCOS process are illustrated in Fig. 1. First, a thin pad oxide (also called stress-relief oxide) is grown on the silicon surface, followed by the deposition and patterning of a silicon nitride layer to mask (i.e., to define) the active areas (Fig. 1(a)). The thin pad oxide underneath the silicon nitride layer is used to protect the silicon surface from stress caused by nitride during the subsequent process steps. The exposed areas of the silicon surface, which will eventually form the isolation regions, are doped with a p-type impurity to create the channel-stop implants that surround the transistors (Fig. 1(b)). Next, a thick field oxide is grown in the areas not covered with silicon nitride, as shown in Fig. 1(c). Notice that the field oxide is partially recessed into the surface since the thermal oxidation process also consumes some of the silicon. Also, the field oxide forms a lateral extension under the nitride layer, called the *bird's beak* region. This lateral encroachment is mainly responsible for a reduction of the active area. The silicon nitride layer and the thin pad oxide layer are etched in the final step (Fig. 1(d)), resulting in active areas surrounded by the partially recessed field oxide. The LOCOS process is a popular technique used for achieving field oxide isolation with a more planar surface topology.-Several additional measures have also been developed over the years to control the lateral bird's beak encroachment, since this encroachment ultimately limits device scaling and device density in VLSI circuits.

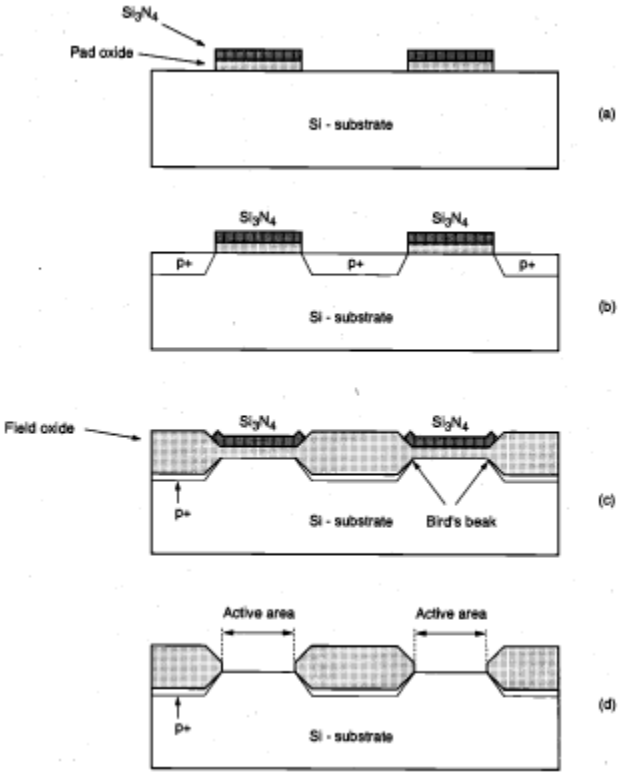


Fig.1. Basic steps of LOCOS Process

11. What are the rules for stick diagrams in VLSI?

ANS:

Stick diagram acts like an interface between circuit diagram and layout diagram which helps in conveying layer information through colour codes.

Rules to be followed are:

1. If the same layer cross each other, it makes a contact.
2. If the different layer just cross, it doesn't make contact but if contact has to be made, it must be indicated explicitly, in the form of dark shaded circle.

3. If a polysilicon cross n- type of diffusion, then nMOS enhancement transistor is formed, if a polysilicon cross n-type of diffusion along with an implant, then nMOS depletion type transistor is formed and if a polysilicon cross n-type of diffusion, PMOS enhancement transistor is formed.
4. PMOS devices must be placed in the pull up part(above demarcation line) and NMOS devices in pull down part(below demarcation line) in CMOS design style.
5. In order to differentiate between the p and n-type devices, demarcation line is used in between the two types.
6. Cross mark has to be used on Vdd and Vss rails in order to create n-well and p-well contact for PMOS devices and NMOS devices respectively.

12. Draw the stick diagram of CMOS inverter with schematic diagram.

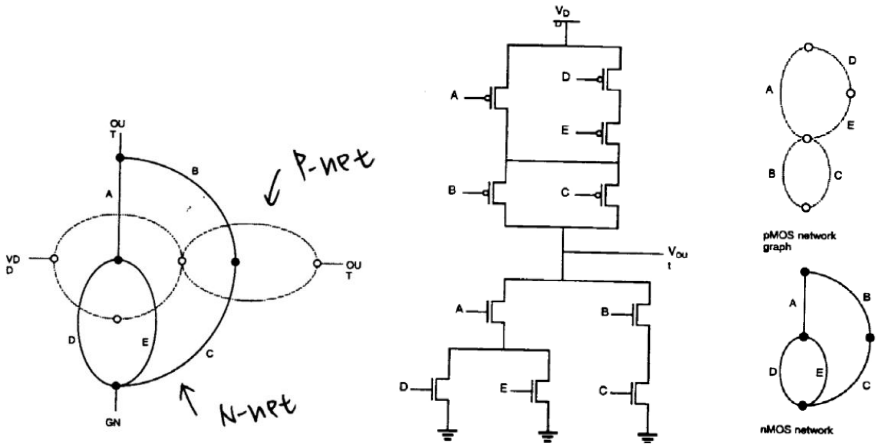
Ans. CMOS Inverter

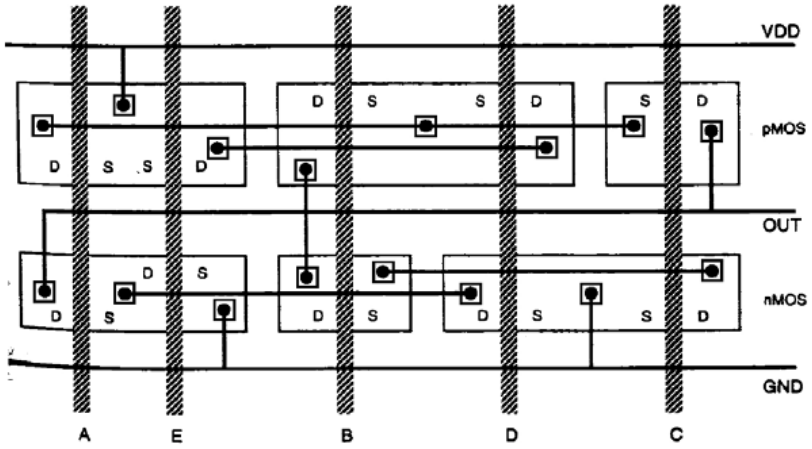
13. Draw the CMOS NOR gate and stick diagram.

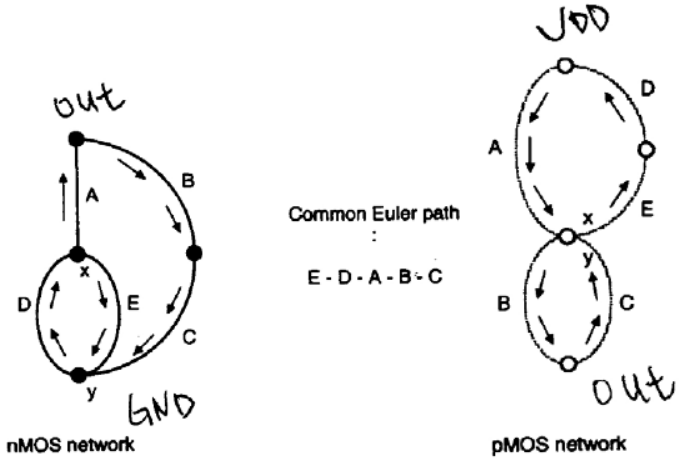
14. Draw the schematic and stick diagram of Y=$\overline{(A.B)+C}$.

15. Draw the schematic and stick diagram of

using Euler path approach

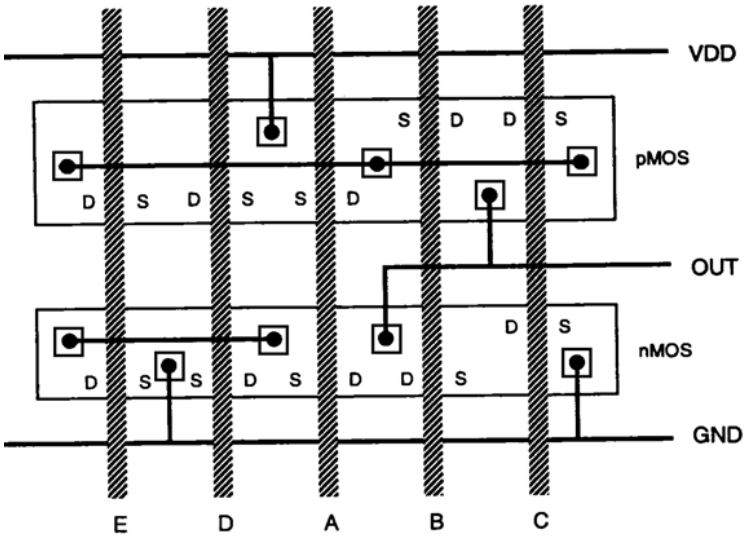






Apply Euler path, find a common Euler path for both graphs .The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once. In both cases, the Euler path starts at (x) and ends at (y).

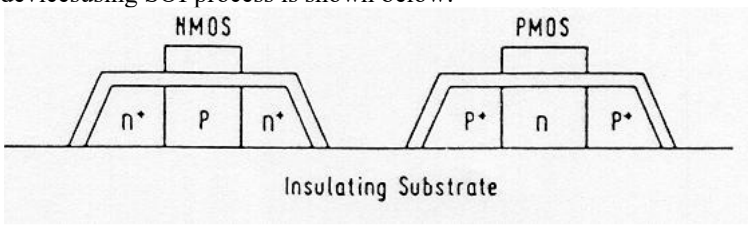
Order = *E,D,A,B,C*



16. What is SOI Process of CMOS Fabrication?

Ans:

Rather than using silicon as the substrate material, technologists have sought to use an insulating substrate to improve process characteristics such as speed and latch-up susceptibility. The SOI CMOS technology allows the creation of independent, completely isolated nMOS and pMOS transistors virtually side-by-side on an insulating substrate. The main advantages of this technology are the higher integration density (because of the absence of well regions), complete avoidance of the latch-up problem, and lower parasitic capacitances compared to the conventional p & n-well or twin tub CMOS processes. The SOI CMOS process is considerably more costly than the standard p & n-well CMOS process. Yet the improvements of device performance and the absence of latch-up problems can justify its use, especially for deep-sub-micron devices. A cross-section of nMOS and pMOS devicesusing SOI process is shown below.



17. Compare the CMOS and BICMOS technology.

Ans:

- The BiCMOS gates perform in the same manner as the CMOS inverter in terms of power consumption, because both gates display almost no static power consumption.
- When comparing BiCMOS and CMOS in driving small capacitive loads, their performance are comparable, however, making BiCMOS consume more power than CMOS.
- On the other hand, driving larger capacitive loads makes BiCMOS in the advantage of consuming less power than CMOS, because the construction of CMOS inverter chains are needed to drive large capacitance loads, which is not needed in BiCMOS.
- The BiCMOS inverter exhibits a substantial speed advantage over CMOS inverters, especially when driving large capacitive loads. This is due to the bipolar transistor's capability of effectively multiplying its current.
- For very low capacitive loads, the CMOS gate is faster than its BiCMOS counterpart due to small values of C_{int}. This makes BiCMOS ineffective when it comes to the implementation of internal gates for logic structures such as ALUs, where associated load capacitances are small.
- BiCMOS devices have speed degradation in the low supply voltage region and also BiCMOS is having greater manufacturing complexity than CMOS.

18. Explain λ-based Design Rules in VLSI circuit Design.

- *Lambda-based* (scalable CMOS) design rules define scalable rules based on λ (which is half of the minimum channel length) – classes of MOSIS SCMOS rules: SUBMICRON, DEEPSUBMICRON
- Stick diagram is a draft of real layout, it serves as an abstract view between the schematic and layout.

- Circuit designer in general want tighter, smaller layouts for improved performance and decreased silicon area. On the other hand, the process engineer wants design rules that result in a controllable and reproducible process.
- Generally we find there has to be a compromise for a competitive circuit to be produced at a reasonable cost. All widths, spacing, and distances are written in the form

$$\lambda = 0.5 \text{ X minimum drawn transistor length}$$

- Design rules based on single parameter, λ
- Simple for the designer
- Wide acceptance
- Provide feature size independent way of setting out mask
- If design rules are obeyed, masks will produce working circuits
- Minimum feature size is defined as 2 λ
- Used to preserve topological features on a chip
- Prevents shorting, opens, contacts from slipping out of area to be contacted

Rule number	*Description*	*λ-Rule*
	Active area rules	
R1	Minimum active area width	3λ
R2	Minimum active area spacing	3λ
	Polysilicon rules	
R3	Minimum poly width	2λ
R4	Minimum poly spacing	2λ
R5	Minimum gate extension of poly over active	2λ
R6	Minimum poly-active edge spacing (poly outside active area)	1λ
R7	Minimum poly-active edge spacing (poly inside active area)	3λ
	Metal rules	
R8	Minimum metal width	3λ
R9	Minimum metal spacing	3λ
	Contact rules	
R10	Poly contact size	2λ
R11	Minimum poly contact spacing	2λ
R12	Minimum poly contact to poly edge spacing	1λ
R13	Minimum poly contact to metal edge spacing	1λ
R14	Minimum poly contact to active edge spacing	3λ
R15	Active contact size	2λ
R16	Minimum active contact spacing (on the same active region)	2λ
R17	Minimum active contact to active edge spacing	1λ
R18	Minimum active contact to metal edge spacing	1λ
R19	Minimum active contact to poly edge spacing	3λ
R20	Minimum active contact spacing (on different active regions)	6λ

19. Explain the layout design rules and the types of design rules.

Ans:

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature

dimensions, and minimum allowable separations between two such features. The main objective of design rules is to achieve, for any circuit to be manufactured with a particular process, a high overall yield and reliability while using the smallest possible silicon area. The design rules are usually described in two ways:

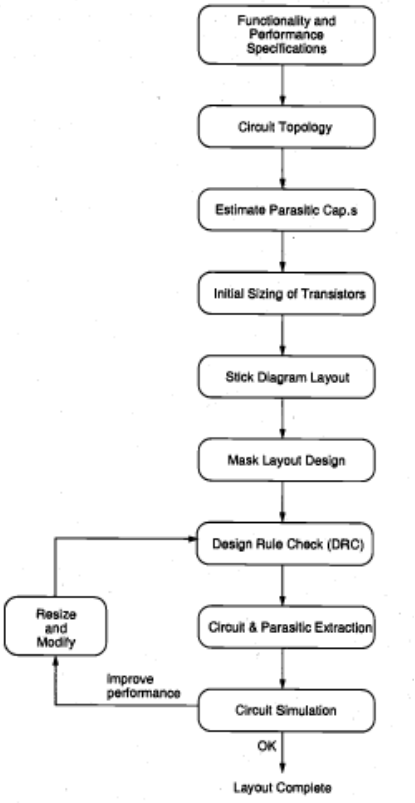
(i) Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers, or,

(ii) Lambda rules, which specify the layout constraints in terms of a single parameter (X) and thus allow linear, proportional scaling of all geometrical constraints.

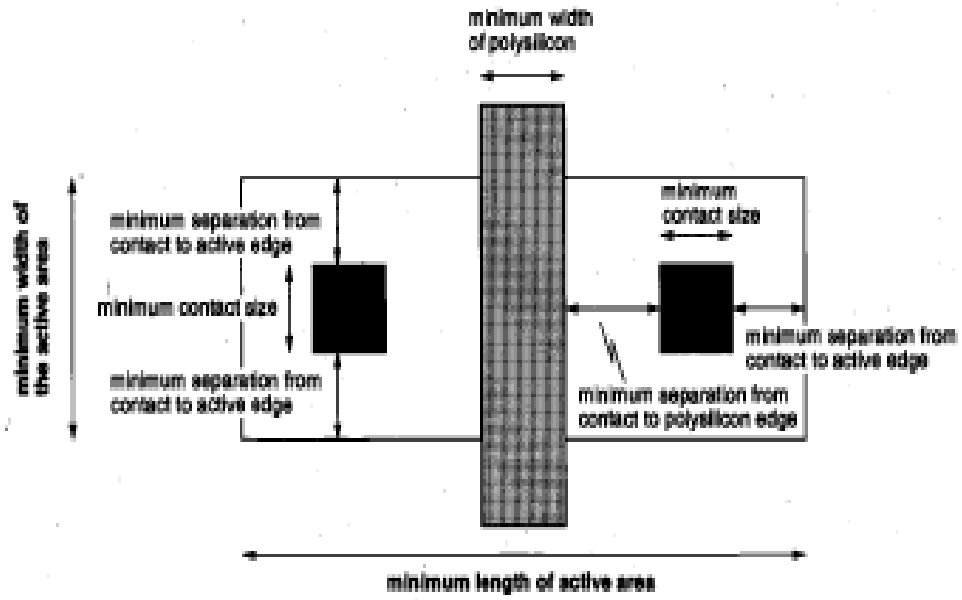
Lambda-based layout design rules were originally devised to simplify the industry standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the submicron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of lambda-based design rules must therefore be handled with caution in submicron geometries.

20. Describe the CMOS layout design for the production of a mask layout.
Ans:

The mask layout design of a CMOS inverter will be examined step-by step, as an example for the application of layout design rules. First, we need to create the individual transistors according to the design rules. Assume that we attempt to design the inverter with minimum-size transistors. The width of the active area is then determined by the minimum diffusion contact size (which is necessary for source and drain connections) and the minimum separation from diffusion contact to both active area edges. The width of the polysilicon line over the active area (which is the gate of the transistor) is typically taken as the minimum poly width (Fig. 2.14). Then, the minimum overall length of the active area is determined by the following sum: (minimum polysilicon width) + 2 x (minimum poly-to-contact spacing) + 2 x (minimum contact size) + 2 x (minimum spacing from contact to active area edge).



Typical design flow for the production of a mask layout.



Design rules which determine the dimensions of a minimum-size transistor.

Chapter -3
MOS Transistor

MULTIPLE CHOICE QUESTIONS:

1. MOS transistor structure is
    a) symmetrical
    b) non symmetrical
    c) semi symmetrical
    d) pseudo symmetrical
2. pMOS is
    a) donor doped
    b) acceptor doped
    c) all of the mentioned
    d) none of the mentioned
3. The condition for linear region is
    a) Vgs lesser than Vt
    b) Vgs greater than Vt
    c) Vds lesser than Vgs
    d) Vds greater than Vgs
4. As source drain voltage increases, channel depth
    a) increases
    b) decreases
    c) logarithmically increases
    d) exponentially increases
5. nMOS devices are formed in
    a) p-type substrate of high doping level
    b) n-type substrate of low doping level
    c) p-type substrate of moderate doping level
    d) n-type substrate of high doping level
6. Source and drain in nMOS device are isolated by
    a) a single diode
    b) two diodes
    c) three diodes
    d) four diodes
7. MOS transistors consists of
    a) semiconductor layer
    b) metal layer
    c) layer of silicon-di-oxide
    d) all of the mentioned
8. In MOS transistors, _____ is used for their gate
    a) metal
    b) silicon-di-oxide
    c) polysilicon
    d) gallium
9. The gate region consists of
    a) insulating layer

b) conducting layer
c) lower metal layer
d) p type layer

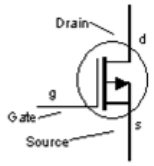
10. Electrical charge flows from
    a) source to drain
    b) drain to source
    c) source to ground
    d) source to gate
11. Source in MOS transistors is doped with _____ material
    a) n-type
    b) p-type
    c) n & p type
    d) none of the mentioned
12. In N channel MOSFET which is the more negative ?
    a) source
    b) gate
    c) drain
    d) source and drain
13. If the gate is given sufficiently large charge, electrons will be attracted to
    a) drain region
    b) channel region
    c) switch region
    d) bulk region
14. Enhancement mode device acts as ____ switch, depletion mode acts as _____ switch
    a) open, closed
    b) closed, open
    c) open, open
    d) close, close
15. Depletion mode MOSFETs are more commonly used as
    a) switches
    b) resistors
    c) buffers
    d) capacitors
16. Which expression is true?
    a) charging time < discharging time
    b) charging time > discharging time
    c) charging time = discharging time
    d) charging time and discharging time are not related
17. In n channel MOSFET, _____ is constant
    a) channel length
    b) channel width
    c) channel depth
    d) channel concentration
18. The conductivity of the pure silicon is raised by :
    a) Introducing Dopants (impurities)

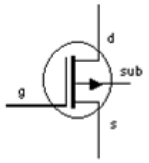
b) Increasing Pressure
c) Decreasing Temperature
d) Deformation of Lattice

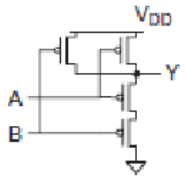
19. The n-type semiconductor have _____ as majority carriers :
a) Holes
b) Negative ions
c) Electrons
d) Positive ions

20. The majority carriers of p-type semiconductor are :
a) Holes
b) Negative ions
c) Electrons
d) Positive ions

21. The n-MOS transistor is made up of:
a) N-type source, n-type drain and p-type bulk
b) N-type source, p-type drain and p-type bulk
c) P-type source, n-type drain and n-type bulk
d) P- type source, p-type drain and n-type bulk

22. The correct representation of n-MOSFET is:
a)


b)


c)


d) None of the mentioned

23. The oxide layer formed in the MOSFET is :
a) Metal oxide
b) Silicon dioxide
c) Poly Silicon oxide
d) Oxides of Non metals

24. The drain current is varied by:
a) Gate to source voltage
b) Gate current
c) Source Voltage
d) None of the mentioned

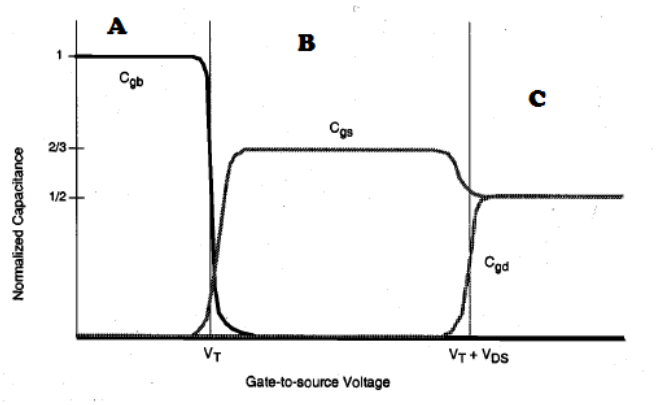
25. The low voltage on the gate of p-MOSFET forms :
    a) Channel of negative carriers
    b) Channel is not formed
    c) Channel is clipped
    d) Channel of positive carriers
26. The n-MOSFET is working as accumulation mode when:
    a) Gate is applied with positive voltage
    b) Gate is grounded
    c) Gate is applied with negative voltage
    d) Gate is connected to source
27. The p-MOS Transistor is said to be in Saturation mode when:
    a) $V_{dsp} > V_{gsp} - V_{tp}$
    b) $V_{gsp} < V_{dsp} - V_{tp}$
    c) $V_{gsp} > V_{tp}$
    d) $V_{dsp} < V_{gsp} - V_{tp}$
28. The Fermi potential of the p-type MOSFET is :
    a) $\varphi fp = (kT/q)\ln(ND/NA)$
    b) $\varphi fp = (kT/q)\ln(NA/ND)$
    c) $\varphi fp = (kT/q)\ln(NA/ ni)$
    d) $\varphi fp = (kT/q)\ln(N_D/n_i)$
29. The principle of the MOSFET operation is:
    a) Control the conduction of current between the source and the drain, using the potential difference applied at the gate voltage as a control variable
    b) Control the current conduction between the source and the gate, using the electric field applied at the drain voltage as a control variable
    c) Control the current conduction between the PN junction, using the electric field generated by the bias voltage as a control variable
    d) Control the current conduction between the PN junctions, using the electric potential generated by the gate voltage as a control variable.
30. Carrier density is scaled by
    a) α
    b) β
    c) 1
    d) α^2
31. Power dissipation per unit area is scaled by
    a) $1/\alpha$
    b) $1/\beta$
    c) β^2/α^2
    d) α^2/β^2
32. For the constant field model, the scaling factors β and α are related as:
    a) $\beta = \alpha$
    b) $\alpha = 2\beta$
    c) $\beta = 1$
    d) $\beta = \alpha = 0$

33. The basic figures of merit for MOS devices are :
    a) Minimum Feature size
    b) Low Power dissipation
    c) Maximum operational frequency
    d) All of the mentioned
34. Transconductance is independent of
    a) channel width
    b) channel length
    c) material
    d) channel depth
35. When dimensions are scaled down, _____ tends to a constant value
    a) current drive from p-transistors
    b) current drive from n-transistors
    c) voltage drive from p-transistors
    d) voltage drive from n-transistors
36. _____ is used with silicon to satisfy the need for very high speed integrated technology
    a) gallium oxide
    b) gallium arsenide
    c) silicon dioxide
    d) aluminium
37. The gate delay is proportional to:
    a) Ron .Cg
    b) Rs.Cds
    c) Rd.Cgs
    d) Ron.Cox
38. The scaling factor of current density in constant voltage model is:
    a) $1/\alpha^2$
    b) 1
    c) α^2
    d) α^2/β
39. Switching energy per gate is scaled by the factor of:
    a) 1
    b) α^2/β
    c) $1/ \beta.\alpha^2$
    d) α^2
40. The scaling factor similar to scaling factor of power speed product is:
    a) Power dissipation per unit area
    b) Switching Energy
    c) Power dissipation per gate
    d) All of the mentioned
41. Which of the following mainly constitutes the output node capacitance:
    a) Inter electrode capacitance
    b) Stray capacitance
    c) Junction Parasitic capacitance
    d) All of the mentioned

42. The junction parasitic capacitance are produced due to:
    a) Source diffusion regions
    b) Gate diffusion regions
    c) Drain diffusion region
    d) All of the mentioned
43. The amount of parasitic capacitance at the output node is determined by:
    a) Concentration of the impurity doped
    b) Size of the total drain diffusion area
    c) Charges stored in the capacitor
    d) None of the mentioned
44. The dominant component of the total output capacitance in submicron technology is:
    a) Drain diffusion capacitance
    b) Gate oxide capacitance
    c) Interconnect capacitance
    d) Junction parasitic capacitance
45. Which of the following is dominant component in input capacitance?
    a) Gate diffusion capacitance
    b) Gate parasitic capacitance
    c) Gate oxide capacitance
    d) All of the mentioned
46. The total load capacitance is calculated as the sum of:
    a) Drain capacitance in series with input capacitance
    b) Drain capacitance + interconnect capacitance +input capacitance
    c) Drain capacitance + interconnect capacitance – input capacitance
    d) Drain capacitance in parallel with input capacitance
47. The interconnect capacitance is formed by:
    a) Area between the interconnect lines
    b) Interconnect lines between the gates
    c) Inter electrode capacitance of interconnect lines
    d) None of the mentioned
48. The amount of gate oxide capacitance is determined by:
    a) Charges present on the gate
    b) Polarity of the gate
    c) Charges present on the substrate
    d) Area of the gate
49. Zero bias depletion capacitance per unit length at sidewall junctions is given by, (Cj is the zero bias depletion capacitance per unit area):
    a) $(\sqrt{10}).Cj.xj$
    b) $(\sqrt{5}).Cj.xj$
    c) $(\sqrt{10}).Cj.xj^2$
    d) $(\sqrt{10}).Cj.xj^3$
50. The active capacitance is also called as:
    a) Parasitic capacitance
    b) Interconnect capacitance

c) Junction capacitance
d) Diffusion capacitance

51.



In the above graph, the regions marked as A,B,C are:

a) A : Saturation, B : Linear, C : Cut-off
b) A :Cut-off, B : Linear, C : Saturation
c) A : Linear, B : Saturation, C : Cut-off
d) None of the mentioned

52. Interconnect capacitance contributes to the load capacitance when the CMOS inverters are connected in cascade configuration.

a) True
b) False

53. Which of the following parameters are found using load capacitance:

a) Delay time
b) Power consumption
c) Speed of the CMOS logic
d) All of the mentioned

54. In cut-off mode, the value of gate to substrate capacitance is equal to:

a) Cox .(W- L)
b) Cox W/ L
c) Cox* W*L
d) 0

Answer key: 1(a), 2(a), 3(b), 4(b),5(c),6(b), 7(d), 8(c), 9(b),10(a), 11(a), 12(a), 13(b), 14(a), 15(b), 16(b), 17(a), 18(a), 19(c), 20(a), 21(a), 22(b), 23(b), 24(a), 25(d), 26(c), 27(d), 28(d), 29(a), 30(c), 31(d), 32(a), 33(d), 34(b), 35(d), 36(b), 37(a), 38(c), 39(c),40(b),41(c),42(c),43(c),44(c),45(c),46(b),47(b), 48(b), 49(a),50(d),51(b),52(a),53(d), 54(c)

SUBJECTIVE QUESTIONS

1. Explain the working of MOS Transistor.

ANS: Working of a MOSFET

MOSFET consists of a MOS capacitor with two p-n junctions placed closed to the channel region and this region is controlled by gate voltage. To make both the p-n junction reverse biased, substrate potential is kept lower than the other three terminals potential.

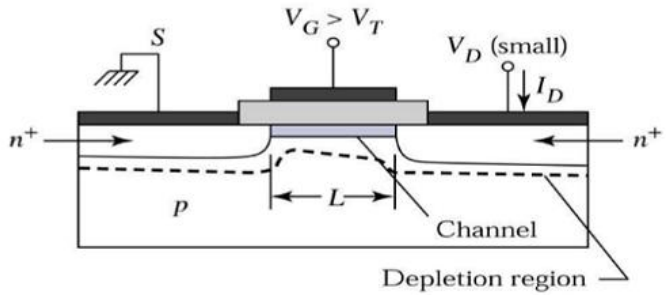
If the gate voltage will be increased beyond the threshold voltage ($V_{GS}>V_{TO}$), inversion layer will be established on the surface and n – type channel will be formed between the source and drain. This n – type channel will carry the drain current according to the V_{DS} value.

For different value of V_{DS}, MOSFET can be operated in different regions as explained below.

Linear Region

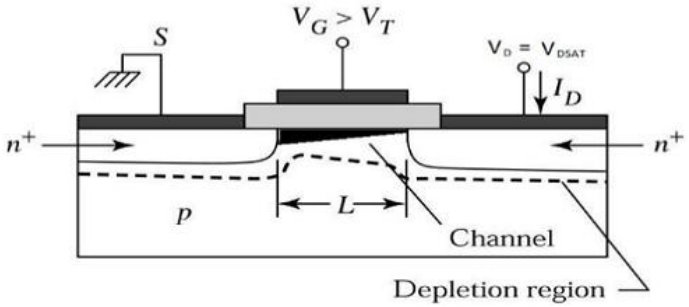
At $V_{DS} = 0$, thermal equilibrium exists in the inverted channel region and drain current $I_D = 0$. Now if small drain voltage, $V_{DS} > 0$ is applied, a drain current proportional to the V_{DS} will start to flow from source to drain through the channel.

The channel gives a continuous path for the flow of current from source to drain. This mode of operation is called **linear region**. The cross sectional view of an n-channel MOSFET, operating in linear region, is shown in the figure given below.



At the Edge of Saturation Region

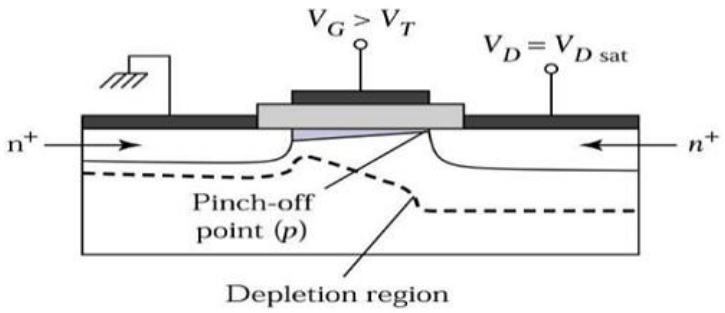
Now if the V_{DS} is increased, charges in the channel and channel depth decrease at the end of drain. For $V_{DS} = V_{DSAT}$, the charges in the channel is reduces to zero, which is called **pinch – off point**. The cross sectional view of n-channel MOSFET operating at the edge of saturation region is shown in the figure given below.



Saturation Region

For $V_{DS}>V_{DSAT}$, a depleted surface forms near to drain, and by increasing the drain voltage this depleted region extends to source.

This mode of operation is called **Saturation region**. The electrons coming from the source to the channel end, enter in the drain – depletion region and are accelerated towards the drain in high electric field.

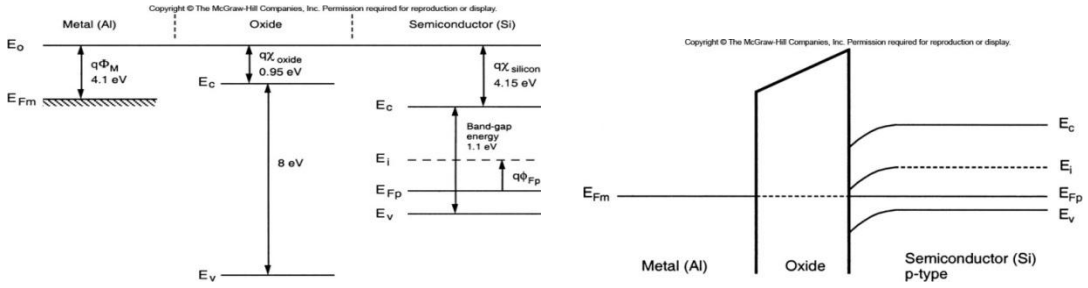


2. Given $q\emptyset_{Fp}$=0.2eV, what is the built in potential in the following MOS structure?

Solution:

We need to find the difference in work functions between the Silicon substrate and the metal gate.

We are given the metal gate work function (4.1eV) so we need to find the Silicon work function:



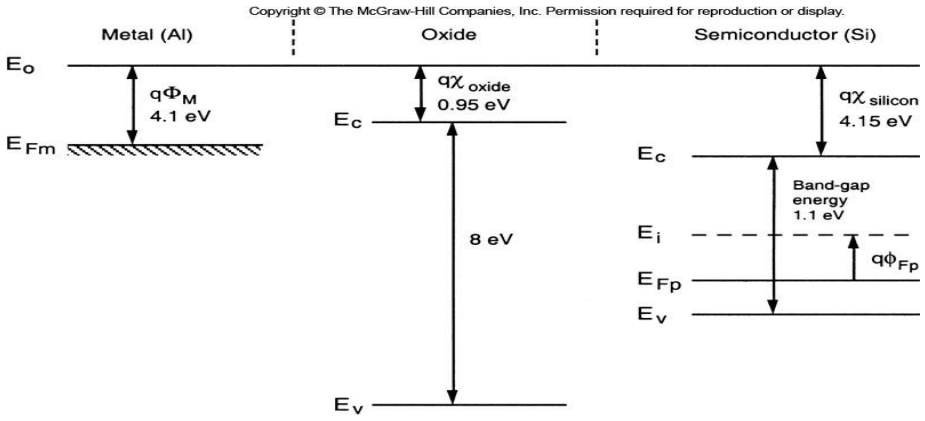
$$q\Phi_S = 4.15eV + \left(\frac{1.1eV}{2} + 0.2eV\right) = 4.9eV$$

Now we just subtract the Silicon work function from the Metal Gate work function:

$$q\Phi_M - q\Phi_S = 4.1eV - 4.9eV = -0.8eV$$

3. Describe the energy band diagram of MOSFET .

Ans:



$q\Phi_M$ = Work Function of Metal

$q\chi_{silicon}$ = Electron affinity of Silicon

$q\chi_{oxide}$ = Electron affinity of Oxide layer

For a p-type semiconductor, the Fermi potential can be approximated by

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{n_i}{N_A}$$

whereas for an n-type semiconductor (doped with a donor concentration *ND),* the Fermi potential is given by

$$\phi_{Fn} = \frac{kT}{q} \ln \frac{N_D}{n_i}$$

Here, k denotes the Boltzmann constant and *q* denotes the unit (electron) charge.

The energy required for an electron to move from the Fermi level into free

space is called the *work function qs,* and is given by

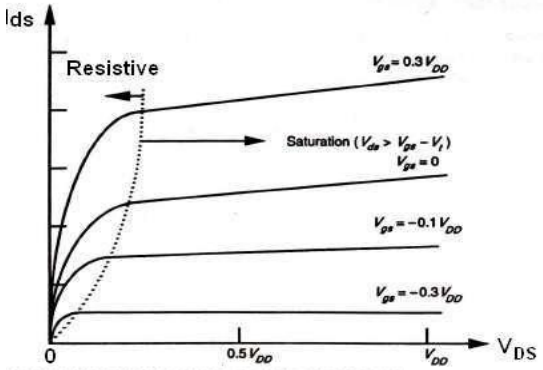
$$q\Phi_S = q\chi + (E_c - E_F)$$

The insulating silicon dioxide layer between the silicon substrate and the gate has a large band-gap of about 8 eV and an electron affinity of about 0.95 eV. On the other hand, the work function q0M of an aluminum gate is about 4.1 eV.

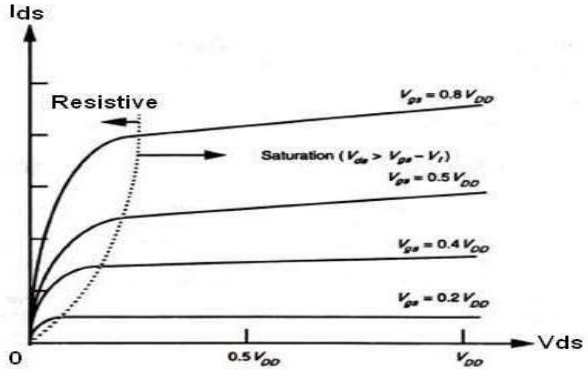
4. Draw the I_D Vs V_{DS} characteristics of MOS Transistor.

Ans:

The graph below shows the ID Vs VDS characteristics of an n- MOS transistor for several values of VGS .It is clear that there are two conduction states when the device is ON. The saturated state and the non-saturated state. The saturated curve is the flat portion and defines the saturation region. For Vgs < VDS + Vth, the nMOS device is conducting and ID is independent of VDS. For Vgs > VDS + Vth, the transistor is in the non-saturation region and the curve is a half parabola. When the transistor is OFF (Vgs < Vth), then ID is zero for any VDS value. The boundary of the saturation/non-saturation bias states is a point seen for each curve in the graph as the intersection of the straight line of the saturated region with the quadratic curve of the non saturated region. This intersection point occurs at the channel pinch off voltage called VDSAT. The diamond symbol marks the pinch-off voltage VDSAT for each value of VGS. VDSAT is defined as the minimum drain-source voltage that is required to keep the transistor in saturation for a given VGS .In the non-saturated state, the drain current initially increases almost linearly from the origin before bending in a parabolic response. Thus the name ohmic or linear for the non-saturated region. source. This is because there is no carrier inversion at the drain region of the channel. Carriers are pulled into the high electric field of the drain/substrate pn junction and ejected out of the drain terminal.



(a) Depletion mode device



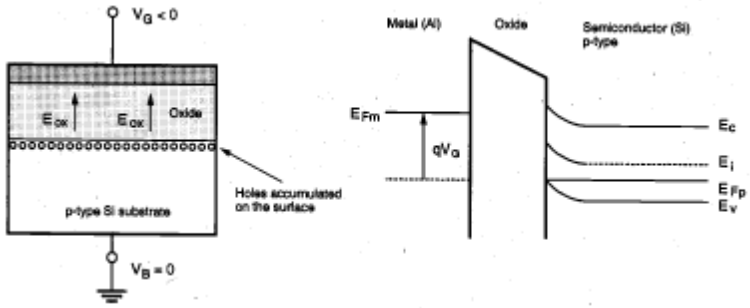
(b). Enhance mode device

5.Explain the MOS system under external bias.

Ans:

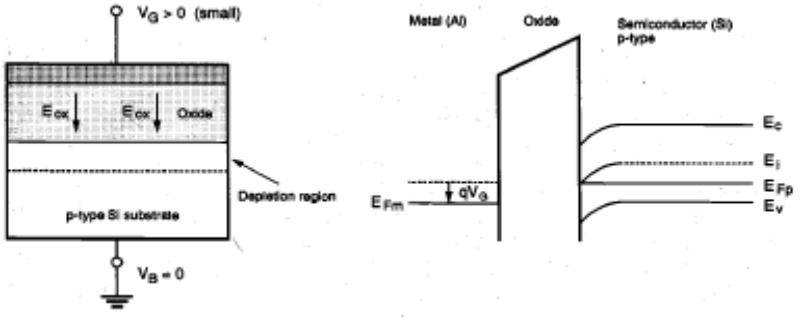
The electrical behavior of the MOS structure under externally applied bias voltages. Assume that the substrate voltage is set at $VB = 0$, and let the gate voltage be the controlling parameter. Depending on the polarity and the magnitude of *VG,* three different operating regions can be observed for the MOS system: accumulation, depletion, and inversion.

a) Accumulation: If a negative voltage *VG* is applied to the gate electrode, the holes in the p-type substrate are attracted to the semiconductor-oxide interface. The majority carrier concentration near the surface becomes larger than the equilibrium hole concentration in the substrate; hence, this condition is called carrier *accumulation* on the surface. the oxide electric field is directed towards the gate electrode. The negative surface potential also causes the energy bands to bend upward near the surface. While the hole density near the surface increases as a result of the applied negative gate bias, the electron (minority carrier) concentration decreases as the negatively charged electrons are pushed deeper into the substrate.



b) Depletion: When a small positive gate bias V_G is applied to the gate electrode. Since the substrate bias is zero, the oxide electric field will be directed towards the substrate in this case. The positive surface potential causes the energy bands to bend downward near the surface. The majority carriers, i.e., the holes in the substrate, will be repelled back into the substrate as a result of the positive gate bias, and these holes will leave negatively charged fixed acceptor ions behind. Thus, a depletion region is created near the surface. The region near the semiconductor-oxide interface is nearly devoid of all mobile carriers. The thickness x_d of this depletion region on the surface can easily be found as a function of the surface potential s. Assume that the mobile hole charge in a thin horizontal layer parallel to the surface is

$$dQ = -q \cdot N_A \cdot dx$$



The *change* in surface potential required to displace this charge sheet d_Q by a distance x_d away from the surface can be found by using the Poisson equation**.**

$$d\phi_s = -x \cdot \frac{dQ}{\varepsilon_{Si}} = \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} dx$$

Integrating the above equation along the vertical dimension (perpendicular to the surface)yields

$$\int_{\phi_F}^{\phi_s} d\phi_s = \int_0^{x_d} \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}}\, dx$$

$$\phi_s - \phi_F = \frac{q \cdot N_A \cdot x_d^2}{2\,\varepsilon_{Si}}$$

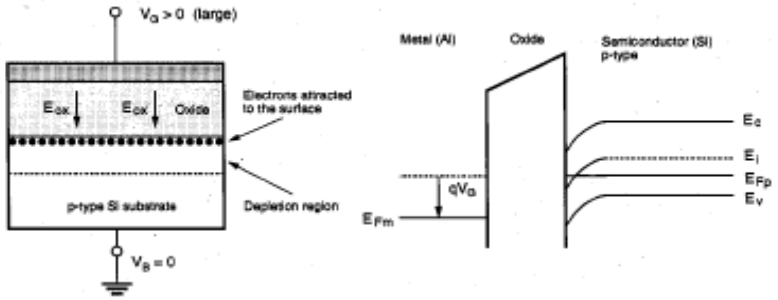
Thus, the depth of the depletion region is

$$x_d = \sqrt{\frac{2\varepsilon_{Si} \cdot |\phi_s - \phi_F|}{q \cdot N_A}}$$

and the depletion region charge density, which consists solely of fixed acceptor ions in this region, is given by the following expression

$$Q = -q \cdot N_A \cdot x_d = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |\phi_s - \phi_F|}$$

c) Inversion: When the gate voltage is increased further then inversion will take place. As a result of the increasing surface potential, the downward bending of the energy bands will increase as well. Eventually, the mid-gap energy level Ei becomes smaller than the Fermi level *EFP* on the surface, which means that the substrate semiconductor in this region becomes n-type. Within this thin layer, the electron density is larger than the majority hole density, since the positive gate potential attracts additional minority carriers (electrons) from the bulk substrate to the surface The n-type region created near the surface by the positive gate bias is called the inversion layer, and this condition is called *surface inversion.* It will be seen that the thin inversion layer on the surface with a large mobile electron concentration can be utilized for conducting current between two terminals of the MOS transistor.

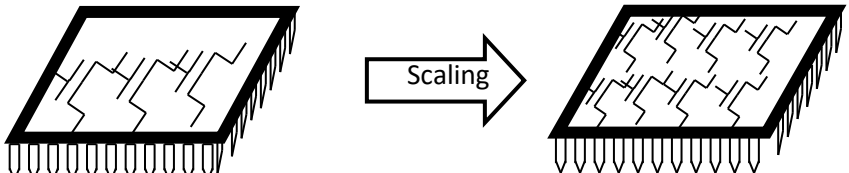


The surface is said to be *inverted* when the density of mobile electrons on the surface becomes equal to the density of holes in the bulk (p-type) substrate. This condition requires that the surface potential has the same magnitude, but the reverse polarity, as the bulk Fermi potential Φ_F. Once the surface is inverted, any further increase in the gate voltage leads to an increase of mobile electron concentration on the surface, but not to an increase of the depletion depth. Thus, the depletion region depth achieved at the onset of surface inversion is also equal to the maximum depletion depth, x_{dm}, which remains constant for higher gate voltages. Using the inversion condition $\Phi s = -\Phi_F$, the maximum depletion region depth at the onset of surface inversion can be found from the equation as follows:

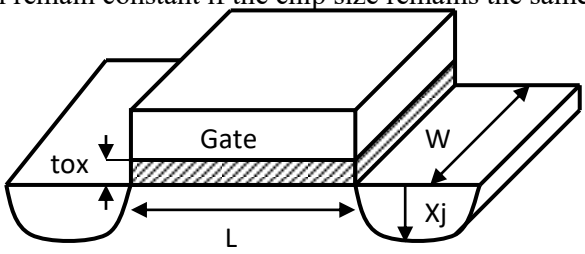
$$x_{dm} = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot |2\phi_F|}{q \cdot N_A}}$$

6. Describe MOSFET Scaling and types of scaling.

Ans:



- To increase the number of devices per IC, the device dimensions had to be shrunk from one generation to another (i.e. scaled down)
- In theory, there are two methods of scaling:
    1. Full-Scaling (also called Constant-Field scaling): In this method the device dimensions (both horizontal and vertical) are scaled down by 1/S, where S is the scaling factor. In order to keep the electric field constant within the device, the voltages have to be scaled also by 1/S such that the ratio between voltage and distance (which represents the electric field) remain constant. The threshold voltage is also scaled down by the same factor as the voltage to preserve the functionality of the circuits and the noise margins relative to one another. As a result of this type of scaling the currents will be reduced and hence the total power per transistor (P=IxV) will also be reduced, however the power density will remain constant since the number of transistors per unit area will increase. This means that the total chip power will remain constant if the chip size remains the same (this usually the case).



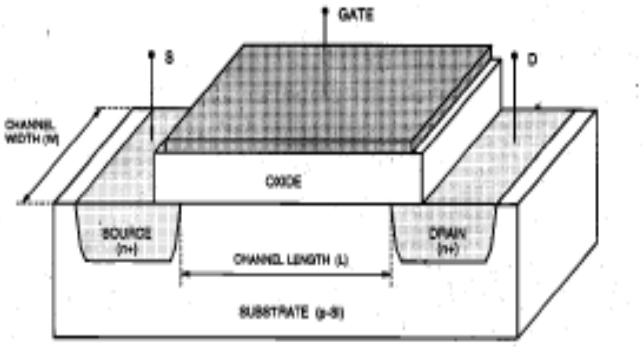
The table below summarizes how each device parameter scales with S (S>1)

Parameter	Before scaling	After scaling
Channel length	L	L/S
Channel width	W	W/S
Oxide thickness	tox	tox/S
S/D junction depth	Xj	Xj/S
Power Supply	VDD	VDD/S
Threshold voltage	V_{TO}	V_{TO} /S
Doping Density	N_A & N_D	N_A *S and N_D *S
Oxide Capacitance	Cox	S*Cox
Drain Current	I_{DS}	I_{DS} /S
Power/Transistor	P	P/S^2
Power Density/cm^2	*p*	*p*

    1. Constant-Voltage scaling (CVS): In this method the device dimensions (both horizontal and vertical are scaled by S, however, the operating voltages remain constant. This means that the electric fields within the device will increase (filed =Voltage/distance). The threshold voltages remain constant while the power per transistor will increase by S. The power density per unit area will increase by S^3. This means that for the same chip area, the power chip power will increase by S^3. This makes constant-voltage-scaling (CVS) very impractical. Also, the device doping has to be increased more aggressively (by S^2) than the constant-field scaling to prevent channel punch-through. Channel punch-through occurs when the Source and Drain Depletion regions touches one another. By increasing the doping by S^2, the depletion region thickness is reduced by S (the same ratio as the channel length). However, there is a limit for how much the doping can be increased (the solid solubility limit of the dopant in Silicon). Again, this makes the CVS impractical in most cases. The following table summarizes the changes in key device parameters under constant-voltage scaling.

Parameter	Before scaling	After scaling
Channel length	L	L/S
Channel width	W	W/S
Oxide thickness	tox	tox/S
S/D junction depth	Xj	Xj/S
Power Supply	VDD	VDD
Threshold voltage	V_{TO}	V_{TO}
Doping Density	N_A & N_D	$N_A * S^2$ and $N_D * S^2$
Oxide Capacitance	Cox	S*Cox
Drain Current	I_{DS}	$I_{DS} * S$
Power/Transistor	P	P*S
Power Density/cm^2	*p*	$p * S^3$

7. Explain briefly the structure of MOSFET and its operating principle.
Ans.

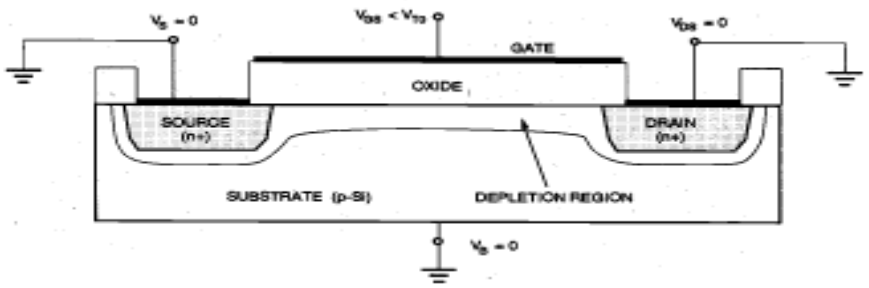


The structure of an n-MOS is shown in the fig above.This is a p-type substrate in which two n+ diffusion regions i.e drain and source are formed. Between the source and drain the surface of the substrate region is covered with a thin oxide layer. Also on the top of the gate dielectric polysilicon gate is deposited.The function of the two n+ regions is to conduct current to this device.A conducting channel will be formed through applied gate voltage between drain and source. The distance between the source and the drain diffusion regions is the channel length L, and the lateral extent of the channel is the channel width W.

The principle of operation of the MOSFET is to control the current conduction between source and drain using the electric field generated by the gate voltage as a control variable.

8. Explain the operation of n – enhancement type MOSFET.
Ans:

The simplest bias condition that can be applied to the n-channel enhancement-type MOSFET is shown in Fig: below. The source, the drain, and the substrate terminals are all connected to ground. A positive gate-to-source voltage *VGS* is then applied to the gate in order to create the conducting channel underneath the gate. For small gate voltage levels, the majority carriers (holes) are repelled back into the substrate, and the surface of the p-type substrate is depleted. Since the surface is devoid of any mobile carriers, current conduction between the source and the drain is not possible.



Now assume that the gate-to-source voltage is further increased. As soon as the surface potential in the channel region reaches - *F* surface inversion will be established, and a conducting n-type layer will form between the source and the drain diffusion regions . This channel now provides an electrical connection between the two n+ regions, and it allows current flow, as long as there is a potential difference between the source and the drain terminal voltages. The bias conditions for the onset of surface inversion and for the creation of the conducting channel are therefore very significant for MOSFET operation.

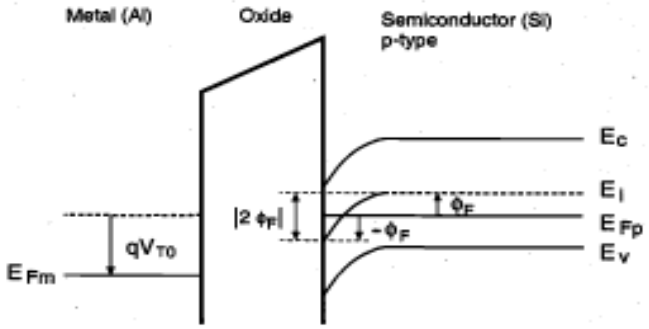


Fig: Band diagram of MOS Structure

The value of the gate-to-source voltage *VGS* needed to cause surface inversion (to create the conducting channel) is called the *threshold voltage V.* Any gate-to-source voltage smaller than V_{TO} is not sufficient to establish an inversion layer; thus, the MOSFET can conduct no current between its source and drain terminals unless $V_{GS} > V_T$. For gate-to-source voltages larger than the threshold voltage, on the other hand, a larger number of minority carriers (electrons) are attracted to the surface, which ultimately contribute to channel current conduction. Also note that increasing the gate to- source voltage above and beyond the threshold voltage will not affect the surface potential and the depletion region depth. Both quantities will remain approximately constant and equal to their values attained at the onset of surface inversion.

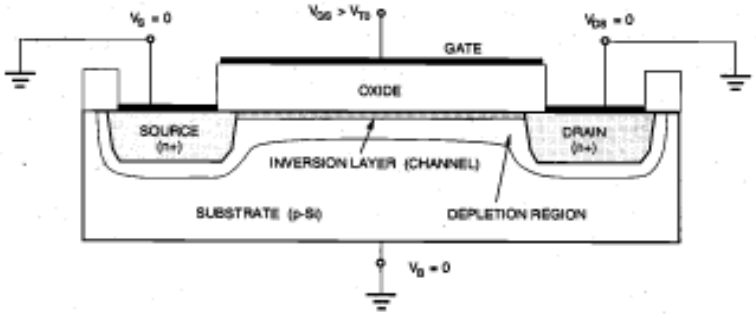


Fig: Formation of an inversion layer (channel) in an n-channel enhancement-type MOSFET.

9. Derive an expression for threshold voltage for n-channel enhancement type MOSFET.
Ans:
The physical parameters affecting the threshold voltage of a MOS structure will be examined by considering the various components of V_{TO}. For all practical purposes, we can identify four physical components of the threshold voltage:
(i) The work function difference between the gate and the channel,
(ii) The gate voltage component to change the surface potential,
(iii) The gate voltage component to offset the depletion region charge, and
(iv) The voltage component to offset the fixed charges in the gate oxide and in the silicon-oxide interface.

(i) The work function difference Φ_{GC} between the gate and the channel reflects the built-in potential of the MOS system, which consists of the p-type substrate, the thin silicon dioxide layer, and the gate electrode. Depending on the gate material, the work function difference is

$\Phi_{GC} = \phi_F(substrate) - \phi_M$ for metal gate
$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate)$ for polysilicon gate

This first component of the threshold voltage accounts for part of the voltage drop across the MOS system that is built-in.
(ii)Now, the externally applied gate voltage must be changed to achieve surface inversion, i.e. to change the surface potential by - $2\Phi_F$. This will be the second component of the threshold voltage. Another component of the applied gate voltage is necessary to offset the depletion region charge, which is due to the fixed acceptor ions located in the depletion region near the surface. We can calculate the depletion region charge density at surface inversion ($\Phi_S = \Phi_F$)

$$Q_{B0} = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |-2\phi_F|}$$

Note that if the substrate (body) is biased at a different voltage level than the source, which is at ground potential (reference), then the depletion region charge density can be expressed as a function of the source-to-substrate voltage V_{SB}.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

(iii) The component that offsets the depletion region charge is then equal to - Q_B/C_{OX}, where C_{ox} is the gate oxide capacitance per unit area.
(iv) The gate voltage component that is necessary to offset this positive charge at the interface is - Q_{OX}/C_{ox}

We can combine all of these voltage components to find the threshold voltage. For zero substrate bias, the threshold voltage V_{TO} is expressed as follows:

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

For nonzero substrate bias, on the other hand, the depletion charge density term must be modified to reflect the influence of V_{SB} upon that charge, resulting in the following generalized threshold voltage expression.

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

The generalized form of the threshold voltage can also be written as

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B - Q_{B0}}{C_{ox}} = V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

10. What is body effect . Write an expression for body effect coefficient.
Ans:

All MOS transistors are usually fabricated on a common substrate and substrate (body) voltage of all devices is normally constant. However, as we shall see in subsequent chapters, when circuits are realized using a number of MOS devices, several devices are connected in series. This results in different source potentials for different devices. It may be noted that the threshold voltage Vt is not constant with respect to the voltage difference between the substrate and the source of the MOS transistor. This is known as the substrate-bias effect or body effect. Increasing the Vsb causes the channel to be depleted of charge carries and this leads to increase in the threshold voltage. Body effect refers to the change in the transistor threshold voltage (V_T) resulting from a voltage difference between the transistor source and body.

The generalized form of the threshold voltage can also be written as

$$V_T = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_B - Q_{B0}}{C_{ox}} = V_{T0} - \frac{Q_B - Q_{B0}}{C_{ox}}$$

$$\frac{Q_B - Q_{B0}}{C_{ox}} = -\frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{ox}} \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

Thus, the most general expression of the threshold voltage V_T can be found as follows:

$$V_T = V_{T0} + \gamma \cdot \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

where the parameter γ

$$\gamma = \frac{\sqrt{2q \cdot N_A \cdot \varepsilon_{Si}}}{C_{ox}}$$

is the substrate-bias (or body-effect) coefficient.

11. Calculate the threshold voltage V_{TO} at V_{SB}= 0, for a polysilicon gate n-channel MOS transistor, with the following parameters: substrate doping density N_A = 10^{16} cm^{-3} , polysilicon gate doping density N_D = 2 x 10^{20} cm^{-3}, gate oxide thickness t_x = 500 Å, and oxide-interface fixed charge density N = 4 x 10^{10} cm^{-2}. First, calculate the Fermi potentials for the p-type substrate and for the n-type polysilicon gate.

Solution:

First, calculate the Fermi potentials for the p-type substrate and for the n-type polysilicon gate:

$$\phi_F(substrate) = \frac{kT}{q} \ln\left(\frac{n_i}{N_A}\right) = 0.026\ \text{V} \cdot \ln\left(\frac{1.45 \cdot 10^{10}}{10^{16}}\right) = -0.35\ \text{V}$$

Φ_F(gate)= 0.55 V.

$$\Phi_{GC} = \phi_F(substrate) - \phi_F(gate) = -0.35\ \text{V} - 0.55\ \text{V} = -0.90\ \text{V}$$

$$Q_{B0} = -\sqrt{2 \cdot q \cdot N_A \cdot \varepsilon_{Si} \cdot |-2\phi_F(substrate)|}$$
$$= -\sqrt{2 \cdot 1.6 \cdot 10^{-19} \cdot 10^{16} \cdot 11.7 \cdot 8.85 \cdot 10^{-14} |-2 \cdot 0.35|} = -4.82 \cdot 10^{-8}\ \text{C/cm}^2$$

$$Q_{ox} = q \cdot N_{ox} = 1.6 \cdot 10^{-19}\ \text{C} \times 4 \cdot 10^{10}\ \text{cm}^{-2} = 6.4 \cdot 10^{-9}\ \text{C/cm}^2$$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.97 \cdot 8.85 \cdot 10^{-14}\ \text{F/cm}}{500 \cdot 10^{-8}\ \text{cm}} = 7.03 \cdot 10^{-8}\ \text{F/cm}^2$$

$$V_{T0} = \Phi_{GC} - 2\phi_F(substrate) - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$
$$= -0.90 - (-0.70) - (-0.69) - 0.09 = 0.40\,\text{V}$$

12. What is the effect of substrate bias on the threshold voltage of the MOS transistor?

Ans.

In many digital circuit applications the source potential of an nMOS transistor can be larger than the substrate potential, which results in a positive source-to-substrate voltage $V_{SB} > 0$. In this case, the influence of the nonzero V_{SB} upon the current characteristics must be accounted for. Recall that the general expression for the threshold voltage V_T already includes the substrate bias term and, hence, it reflects the influence of the nonzero source-to-substrate voltage upon the device characteristics.

$$V_T(V_{SB}) = V_{T0} + \gamma \cdot \left(\sqrt{|2\phi_F| + V_{SB}} - \sqrt{|2\phi_F|}\right)$$

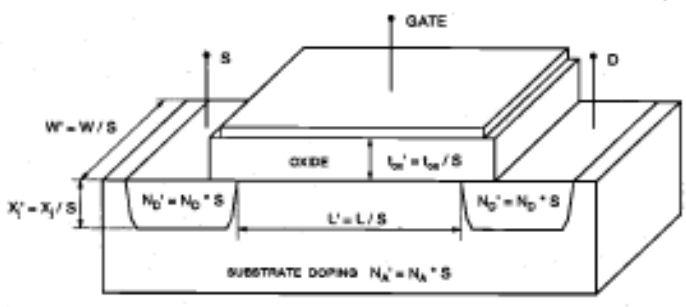
Here γ is called channel length modulation coefficient.
Therefore

$$I_D(lin) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot \left(V_{GS} - V_T(V_{SB})\right)V_{DS} - V_{DS}^2\right]$$

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left(V_{GS} - V_T(V_{SB})\right)^2 \cdot (1 + \lambda \cdot V_{DS})$$

A higher potential needs to be applied to the gate in order to bend the bands by the same amount in order to create the same electron concentration in the channel.

13. Explain the effect of full scaling on device parameters.
Ans:



This scaling option attempts to preserve the magnitude of internal electric fields in the MOSFET, while the dimensions are scaled down by a factor of S. To achieve this goal, all potentials must be scaled down proportionally, by the same scaling factor. Note that this potential scaling also affects the threshold voltage V_{TO} .Finally, the Poisson equation describing the relationship between charge densities and electric fields dictates that the charge densities must be increased by a factor of S in order to maintain the field conditions. The table below lists the scaling factors for all significant dimensions, potentials, and doping densities of the MOS transistor.

Quantity	Before Scaling	After Scaling
Channel length	L	$L' = L/S$
Channel width	W	$W' = W/S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox}/S$
Junction depth	x_j	$x_j' = x_j/S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD}/S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0}/S$
Doping densities	N_A N_D	$N_A' = S \cdot N_A$ $N_D' = S \cdot N_D$

Q14. What is channel length modulation effect? How the voltage current characteristics are affected because of this effect?

Ans: It is assumed that channel length remains constant as the drain voltage is increased appreciably beyond the onset of saturation. As a consequence, the drain current remains constant in the saturation region. In practice, however the channel length shortens as the drain voltage is increased. For long channel lengths, say more than 5 μm, this variation of length is relatively very small compared to the total length and is of little consequence. However, as the device sizes are scaled down, the variation of length becomes more and more predominant and should be taken into consideration. As a consequence, the drain current increases with the increase in drain voltage even in the saturation region.

Q.15. What are the various ways to reduce the delay time of a CMOS inverter of a CMOS inverter?

Ans: Various ways for reducing the delay time are given below:

(a) The width of the MOS transistors can be increased to reduce the delay. This is known as gate sizing.

(b) The load capacitance can be reduced to reduce delay. This is achieved by using transistors of smaller and smaller dimensions as provided by future generation technologies.

(c) Delay can also be reduced by increasing the supply voltage V_{dd} and/or reducing the threshold voltage Vt of the MOS transistors.

MOS INVERTER-STATIC CHARACTERISTICS

MULTIPLE CHOICE QUESTIONS

1. CMOS inverter has _____ regions of operation
a) three
b) four
c) two
d) five

2. If n-transistor conducts and has large voltage between source and drain, then it is said to be in _____ region
a) linear
b) saturation
c) non saturation
d) cut-off

3. If p-transistor is conducting and has small voltage between source and drain, then the it is said to work in
a) linear region
b) saturation region
c) non saturation resistive region
d) cut-off region

4. In the region where inverter exhibits gain, the two transistors are in _____ region
a) linear
b) cut-off
c) non saturation
d) saturation

5. If both the transistors are in saturation, then they act as
a) current source
b) voltage source
c) divider
d) buffer

6. If $\beta n = \beta p$, then Vin is equal to
a) Vdd
b) Vss
c) 2Vdd
d) 0.5Vdd

7. Mobility depends on
a) transverse electric field
b) Vg
c) Vdd
d) Channel length

8. In CMOS inverter, transistor is a switch having
a) infinite on resistance
b) finite off resistance
c) buffer
d) infinite off resistance

9. CMOS inverter has _____ output impedance
a) low
b) high

10. Increasing fan-out, _____ the propagation delay
a) increases
b) decreases
c) does not affect
d) exponentially decreases

11. Fast gate can be built by keeping
a) low output capacitance
b) high on resistance
c) high output capacitance
d) input capacitance does not affect speed of the gate

12. In inverter circuit, _____ transistors is used as load
a) enhancement mode
b) depletion mode
c) all of the mentioned
d) none of the mentioned

13. For depletion mode transistor, gate should be connected to
a) source
b) drain
c) ground
d) positive voltage rail

14. In nMOS inverter configuration depletion mode device is called as
a) pull up
b) pull down
c) all of the mentioned
d) none of the mentioned

15. If p-transistor is conducting and has small voltage between source and drain, then the it is said to work in
a) linear region
b) saturation region
c) non saturation resistive region
d) cut-off region

16. In the region where inverter exhibits gain, the two transistors are in _____ region
a) linear
b) cut-off
c) non saturation
d) saturation

17. If both the transistors are in saturation, then they act as
a) current source
b) voltage source
c) divider
d) buffer

18. In CMOS inverter, transistor is a switch having
a) infinite on resistance
b) finite off resistance
c) buffer
d) infinite off resistance

19. CMOS inverter has _____ output impedance
a) low
b) high

20. Reduction in power dissipation can be brought by
a) increasing transistor area
b) decreasing transistor area
c) increasing transistor feature size
d) decreasing transistor feature size

21. The area of CMOS inverter is proportional to
a) area of n device
b) area of p device
c) total area of n and p device
d) square of minimum feature size

22. Input Voltage between VIH and VOH is considered as:
a) Logic Input 1
b) Logic Input 0
c) Uncertain
d) None of the mentioned

23. MOSFET is used as
a) current source
b) voltage source
c) buffer
d) divider

24. Performance is better if power speed product is
a) low
b) high
c) very low
d) very high

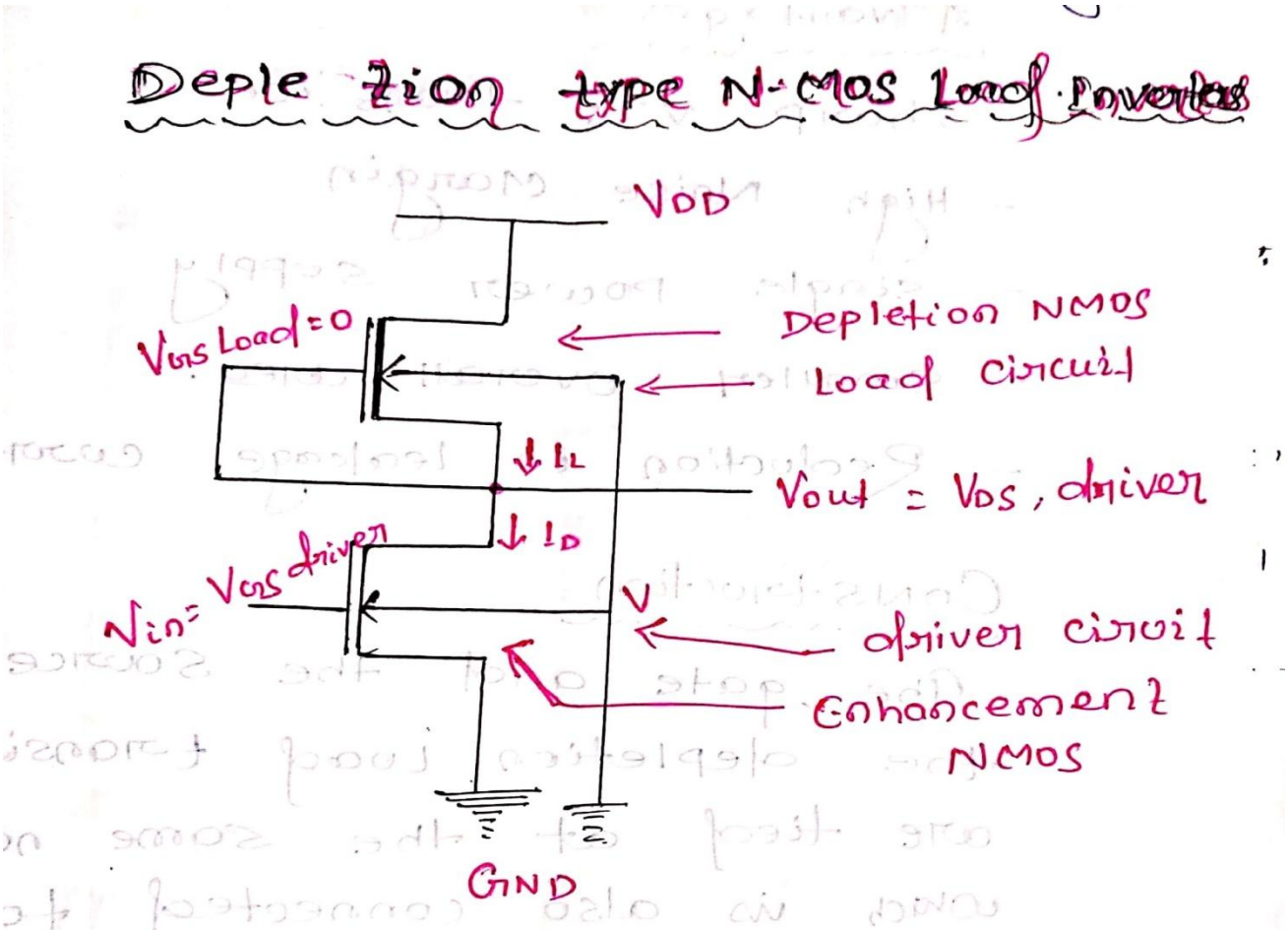
25. Which has better noise margins?
a) nMOS
b) pMOS
c) CMOS
d) BiCMOS

Answer key: 1(d), 2(b), 3(c), 4(d), 5(a), 6(d),7(a),8(b), 9(a),10(a), 11(a),12(b),13(a), 14(a),15(c),16(d),17(a),18(b),19(a), 20(a), 21(c), 22(a), 23(a),24(b),25(c)

SUBJECTIVE QUESTIONS

Q-1 : Derive the expression for saturation drain current and linear drain current equation for depletion type nMOS load inverters.

Ans:



The above ckt shows the implementation of depletion Load inverter in which the driver transister is enhancement mode and the load transister is depletion mode N-MOS.

The fig. shows an inverter consisting of NMOS enhancement type driver ckt and depletion type NMOS load circuit.

$V_{To\,driver} > 0$ &

$V_{To\,(Load} < 0$

Here, $V_{GS\,(Load)} = 0$

Since V_{To} Load is -ve, the condn the $V_{GS\,(Load)} > V_{To\,(Load)}$ is satisfied and the load device always in conduction state. Irrespective of I/P & O/P voltage levels.

Here. $V_{SB\,(Load)} = V_{out}$

So, for a finite V_{SB}

$$V_{T\,(Load)} = V_{To(Load} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right)$$

Replacing V_{SB} by V_{out}

$$= V_{To\,(Load)} + \gamma\left(\sqrt{|1-2\phi_F + V_{out}|} - \sqrt{|2\phi_F|}\right)$$

where,

γ = substrate bias coefficient (body effect)

$$\gamma = \frac{\sqrt{2 q N_A \varepsilon_{Si}}}{C_{ox}}$$

and ϕ_F = fermi potential of substrate.

The operating mode of the load transistor is determined by the o/p voltage level.

- when the o/p voltage is small that is the load transistor draws maxm current which means the transistor is in saturation region.

$$V_{DS(load)} > V_{GS(Load)} - V_{T(Load)}$$

$$\Rightarrow V_{DD} - V_{out} > 0 - V_{T(Load)}$$

{Applying KVL, $V_{DS(load)} = V_{DD} - V_{out}$ and $V_{GS(Load)} = 0$ }

$$\Rightarrow V_{DD} - V_{out} > - V_{T(Load)}$$

$$\Rightarrow \boxed{V_{out} < V_{DD} + V_{T(load)}}$$

↳ condition for load transistor to be in saturation.

The drain current in saturation is given by

$$I_{D(sat)\ load} = \frac{k_n}{2}\left[V_{GS(Load)} - V_{T(Load)} \cdot V_{SB\ Load}\right]^2$$

$$\left[I_D = \frac{k_n}{2}\left(V_{GS} - V_{T_{Load}}\right)^2\right]$$

$$\Rightarrow I_{D(Load)} = \frac{k_{n\,load}}{2}\left[0 - V_{T\,Load} \cdot V_{out}\right]^2$$

$$\Rightarrow I_{D(Load)} = \frac{k_{n(Load)}}{2}\left[-V_{T(Load} \cdot V_{out}\right]^2$$

$$\Rightarrow \boxed{I_{D(Load)} = \frac{k_{n(Load)}}{2}\left|V_{T\,Load} \cdot V_{out}\right|^2}$$

↳ saturation

for larger o/p voltage

$$V_{out} > V_{DD} + V_{T(Load)}$$

. The transistor draw minm current i.e. the transistor operates in linear region.

$$I_{D(Lin)\ Load} = \frac{k_{n(Load)}}{2}\left[2\left(V_{GS(Load)} - V_{T(Load)} \cdot V_{SB(Load)}\right)V_{DS(Load)} - V_{DS(Load)}^2\right]$$

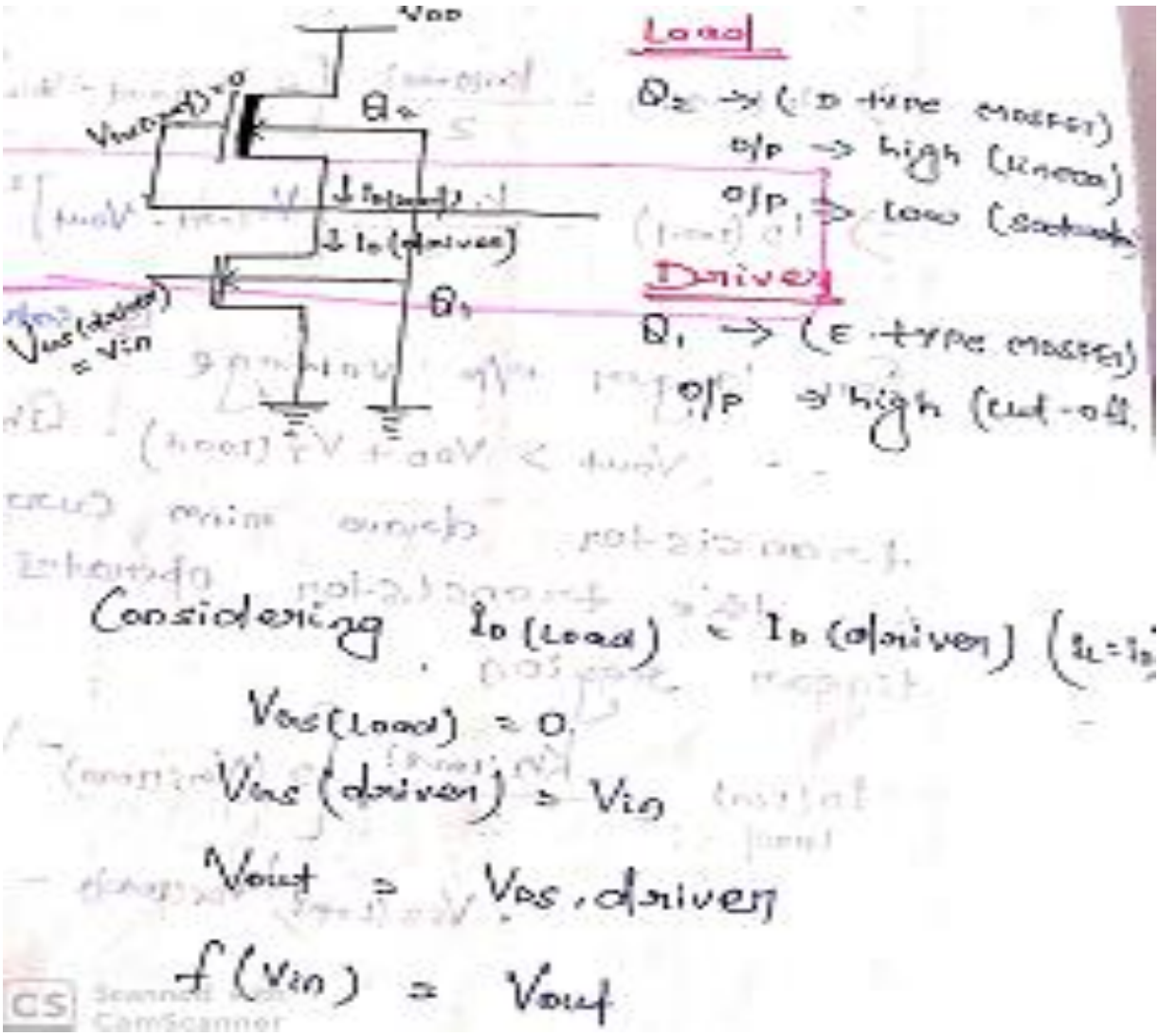
$$= \frac{K_{n(Load)}}{2}\left[2\left(0 - V_{T(Load)} \cdot V_{out}\right)\left(V_{DD} - V_{out}\right) - \left(V_{DD} - V_{out}\right)^2\right]$$

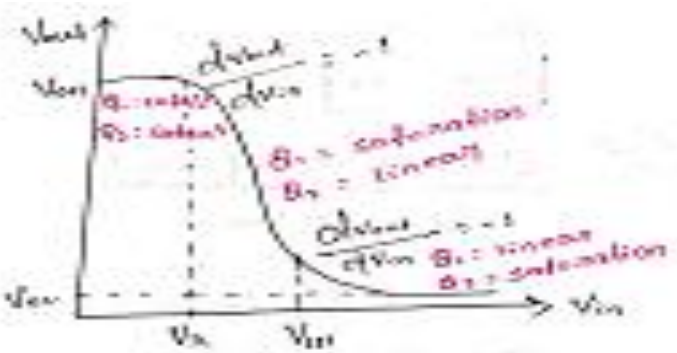
$$I_{D(Load)} = \frac{K_{n(Load)}}{2}\left[2\left|V_{T(Load)}\, V_{out}\right|\left(V_{DD} - V_{out}\right) - \left(V_{DD} - V_{out}\right)^2\right]$$

↳ Linear

Q-2. Find all the critical voltages of a depletion load n MOS inverter .

Ans.





Calculation of V_{OL} :- (o/p is low)

for $V_{out} = V_{OL}$

$V_{GS} < V_{TO}$(driver)

i.e. the driven transistor must be in cut-off and does not conduct any drain current, consequently the load device which operates in linear region has zero drain current. hence

$$I_{D(load)} = \frac{k_{n(load)}}{2}\left[2\left|V_{T(load)}\right| \cdot V_{OL} - V_{OL}^2\right] - (V_{DD} - V_{OL})^2$$

$$= 0$$

The above eqn is true if

$V_{DD} = V_{OH}$

Calculation of V_{OL} :-

V_{OL} = o/p Low

for $V_{out} = V_{OL}$

$V_{in} = V_{DD}$ (maxm) :

The driver transistor in a linear region while the depletion type load transistor is in saturation region.

$$I_{D(driver)} = I_{D(load)}$$

$$\Rightarrow \frac{K_{n(driva)}}{2} \left[2(V_{DD} - V_{TO}) V_{OL} - V_{OL}^2\right]$$

$$= \frac{K_{n(load)}}{2} \left| V_{T(load)} \cdot V_{out} \right|^2$$

Solving

$$V_{OL} = V_{DD} - V_{TO} - \sqrt{(V_{DD} - V_{TO})^2 - \frac{K_{n(load)}}{K_{n(driva)}} \cdot \left| V_{T(load)} \cdot V_{out} \right|^2}$$

Calculation of V_{IL} :-

At $V_{in} = V_{IL}$

when $V_{in} = V_{IL}$ so, $\frac{dV_{out}}{dV_{in}} = -1$

Since V_{in} is the maxm i/p voltage so, the driver transistor operates in the saturation region while the load transistor operates in linear region.

$$I_{D(driver)} = I_{D(load)}$$

$$\Rightarrow \frac{|K_{n(driver)}|}{2}(V_{in}-V_{T_0})^2 = \frac{|K_{n(load)}|}{2}\left[2|V_{T(load)}\cdot V_{OUT}|(V_{DD}-V_{OUT})-(V_{DD}-V_{OUT})^2\right]$$

Differentiating both the side w.r.t. V_{in}

$$\Rightarrow \frac{K_{n(driver)}}{2}\cdot 2(V_{in}-V_{T_0}) = K_{n(load)}\frac{d}{dV}\left[2|V_{T(load)}V_{OUT}|(V_{DD}-V_{OUT})-(V_{DD}-V_{OUT})^2\right]$$

Substituting $V_{in} = V_{IL}$ & $\frac{dV_{OUT}}{dV_{in}} = -1$

Solving, we get

$$V_{IL} = V_{T_0} + \frac{K_{n(load)}}{K_{n(driver)}}\left[V_{OUT}-V_{DD}+|V_{T(load)}V_{OUT}|\right]$$

Calculation of V_{IH} :-

When $V_{in} = V_{IH}$

then, $\frac{dV_{OUT}}{dV_{in}} = -1$ & V_{OUT} is small i.e. equal to V_{OL}.

$$V_{OUT} = V_{OL}$$

∴ The driver transistor is in linear region & load transistor is in saturation.

$$I_{D(driver)} = I_{D(load)}$$

$$\frac{K_{n(driver)}}{2}\left[2(V_{in}-V_{To})V_{out}-V_{out}^2\right] = \frac{K_{n(load)}}{2}\left[-V_{T(load)}\cdot V_{out}\right]^2$$

Differentiating w.r.t. V_{in}.

$$\Rightarrow K_{n(driver)} = \frac{d}{dV_{in}}\left[2(V_{in}-V_{To})V_{out}-V_{out}^2\right] = K_{n(load)}\frac{d}{dV_{in}}\left[-V_{T(load)}\cdot V_{out}\right]^2$$

At $V_{in} = V_{IH}$ & $\frac{dV_{out}}{dV_{in}} = -1$, substituting & solving we get

1- $$V_{IH} = V_{To} + 2V_{out} + \frac{K_{n(load)}}{K_{n(driver)}}\left[-V_{T(load)}V_{out} - \frac{dV_{T(load)}}{dV_{out}}\right]$$

where,

$$\frac{dV_{T(load)}}{dV_{out}} = \frac{\gamma}{2\sqrt{|2\phi_F|+V_{out}}}$$

Q.3: Explain the design parameters of Depletion load nMOS inverter.

Design of Depletion load Inverter :-

→ V_{DD}
→ Threshold voltage
→ W/L ratio

The parameters of inverter ckt are
- power supply voltage V_{DS}
- The threshold voltage of driver and load.
- W/L ratio of driver & load transistor.

Practically the V_{DD} and the threshold voltage of the driver & the load transistor cannot be adjusted for each individual transistor. So, W/L ratio of transistor & driver to load ration (K_R) is the main design parameter.

Rewriting the V_{OL} eqn

$$\Rightarrow \frac{K_{n(driver)}}{2}\left[2(V_{OH}-V_{T0})V_{OL}-V_{OL}^2\right] = \frac{K_{n(load)}}{2}\left[-V_{T(load)}\cdot V_{OL}^2\right]$$

$$\Rightarrow \frac{K_{n(driver)}}{K_{n(load)}} = \frac{\left|-V_{T(load)}\cdot V_{OL}\right|^2}{2(V_{OH}-V_{T0})V_{OL}-V_{OL}^2}$$

$$K_R = \frac{K_{(driver)}}{K_{(Load)}}$$

$$= \frac{(\mu_n C_{ox})_{driver} \left(\frac{W}{L}\right)_{driver}}{(\mu_n C_{ox})_{Load} \left(\frac{W}{L}\right)_{Load}}$$

$$= K_R - \frac{K_n'(driver)}{K_n'(Load)} \cdot \frac{(W/L)_{driver}}{(W/L)_{Load}}$$

If $K_n'(driver) = K_n'(Load)$

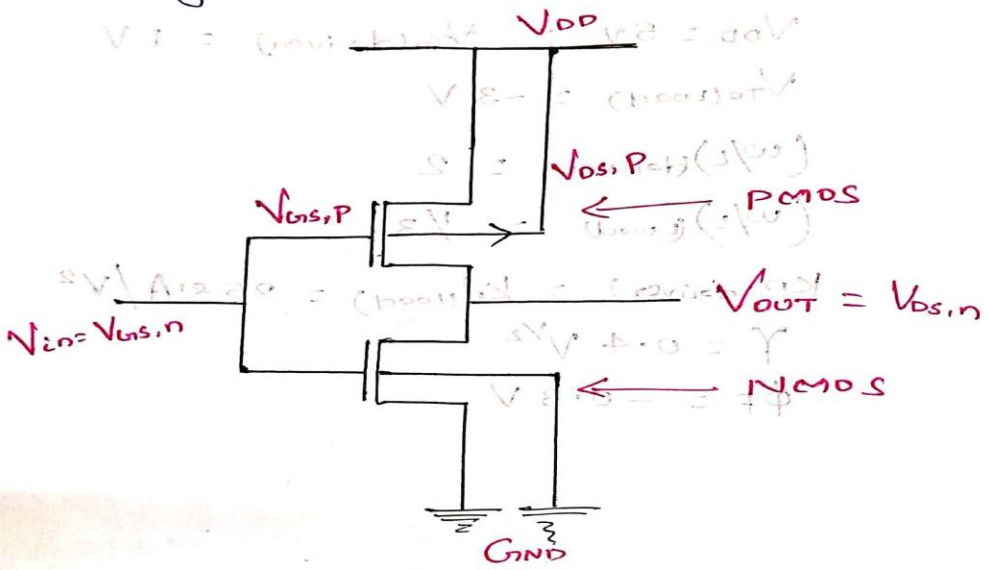
$$K_R = \frac{(W/L)_{driver}}{(W/L)_{Load}}$$

Q-4. Explain the operation of CMOS inverter. What are the advantages of CMOS inverter? Explain the fabrication complexities of CMOS inverter.

Ans:

CMOS INVERTER :-

CMOS inverter is the most basic elt element in digital VLSI design. It is the combination of NMOS and PMOS. so it is called as complimentory MOS transistor (CMOS).



For High I/P the NMOS transistor drives the o/p node while the PMOS transistor acts as a load and for low I/P the PMOS transistor drives the o/p node by while the NMOS transistor behaves as a load

Advantages of cmos inverter:

- We can neglect the steady state power dissipation of cmos inverter ckt except for small power dissipation due to leakage current.
- The VTC also exibits the full o/p voltage swing in betn zero and V_{DD}.
- The transition of VTC is also sharp this makes the VTC of cmos inverter is as like an ideal inverter.

Construction

The cmos ckt consist of enhancement NMOS and enhancement PMOS operating in complementary mode.

It is complementary push pull transistor for high input PMOS act as a load and NMOS act as a driver (pull down)

For low input PMOS acts as a driver and NMOS acts as a load (pull up).

Circuit operation :-

The I/P voltage is connected to both the gate terminals of both PMOS and NMOS.

The substrate bias voltage of PMOS is connected to V_{DD} and NMOS is connected to ground.

If is done so the reverse bias the source and drain function.

The substrate bias affect is neglected for both NMOS & PMOS i.e. $V_{SB} = 0$

Assumption :-

$V_{in} = V_{GS,n}$

$V_{out} = V_{DS,n}$

$V_{GS,P} = -(V_{DD} - V_{in})$

$V_{DS,P} = -(V_{DD} - V_{OUT})$

Let us consider 2 cases.

a) When I/P voltage is low :- (case-1)

When I/P voltage is low, i.e. $V_{in} = 0$. In this case NMOS transistor turns off because $V_{GS,n} = 0V < V_{TO,n}$. The PMOS transistor turns on because $V_{GS,P} = -V_{DD}$

PMOS behaves as a shortckt and NMOS behaves as a open ckt.

$I_{D,n} = I_{D,p} = 0$

The drain to source voltage of PMOS transistor is also equal to zero. The o/p voltage

$V_{OUT} = V_{OH} = V_{DD}$

Here, PMOS is driver and NMOS is load this path is called as pullup path and PMOS is called as pull-up transistor.

Case-2 (when i/p voltage is high): (exceeds $V_{DD} + V_{To,p}$)

For High i/p NMOS turns on because $V_{GS,n} = V_{DD} \geq V_{To,n}$ and PMOS turns off. The NMOS will be operating in the linear region, but its drain to source voltage is equal to zero because

$I_{D,n} = I_{D,p} = 0$

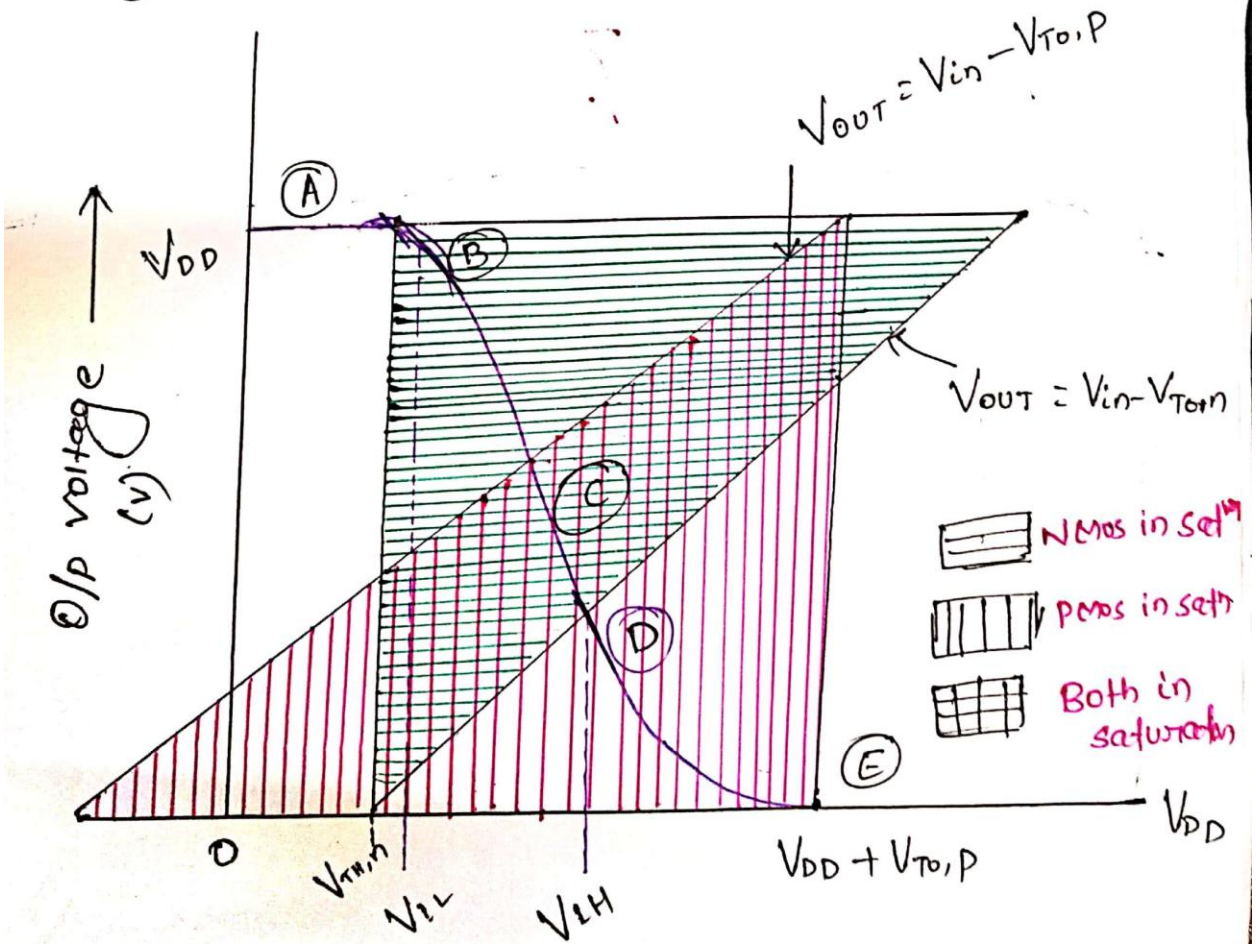
and the o/p voltage is

$V_{OUT} = V_{OL} = 0$

The direct path exists between the o/p and the ground, since no current flows from V_{DD} to o/p.

The voltage drop across the NMOS = 0 i.e. $V_{out} = 0V$. In this case o/p is PULL down to zero. & Hence it is called as PULL-down transistor.

Operating Regions of NMOS & PMOS transistor :-



Fabrication Complexity in

As NMOS and PMOS transistor are fabricated on a single chip side by side the CMOS process becomes more complex.

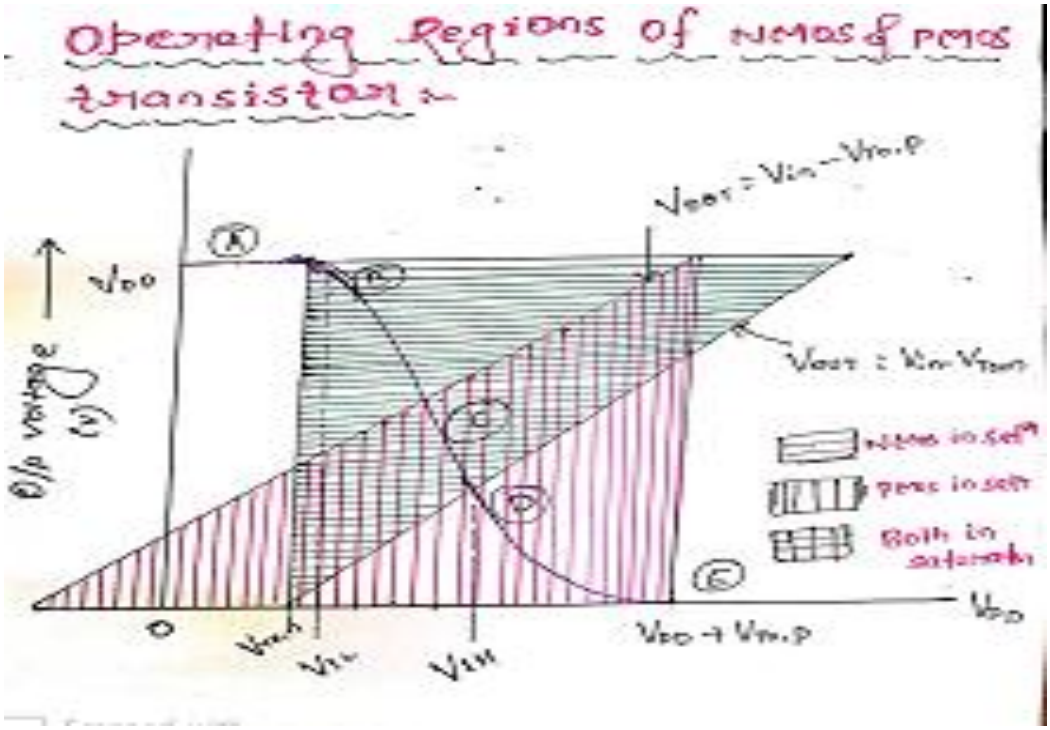
- In the CMOS process an N type substrate is provided for the PMOS transistor and the P type substrate is provided for the NMOS transistor. This is achived by building in an N type tubs (wells) on a P type wafer or by build in P-type tubs on an n-type wafer.

- Due to close proximity between NMOS and PMOS transistors 2-parasitic bipolar transistor are formed and causes a latch up condition.

To prevent the addition guard rings are build around NMOS and PMOS transistor.

Q-5. Explain the operating regions of CMOS inverter .

Ans.



Circuit operation :-

→ The i/p voltages V_{in} is connected to both the gate terminals of the PMOS & NMOS. The substrate bias voltage of NMOS is grounded and PMOS is connected to the V_{DD}. It is done so to reverse bias the source and drain junctions. The substrate bias effect is neglected for nMOS and PMOS because $V_{SB} = 0$.

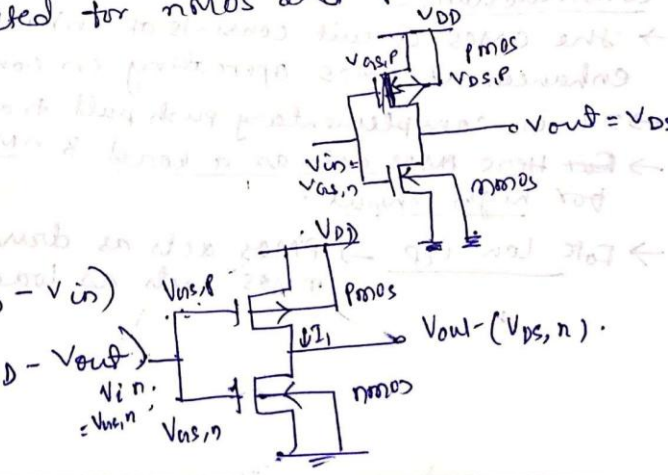
Assumptions :-

$V_{GS,n} = V_{in}$

$V_{DS,n} = V_{out}$

$(V_{GS,P}) = -(V_{DD} - V_{in})$

$(V_{DS,P}) = -(V_{DD} - V_{out})$



Region	V_{in}	V_{out}	nMOS	PMOS
A	$< V_{TO,n}$	V_{OH}	cut off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{TH}	V_{th}	saturation	sat^n.
D	V_{IH}	low $\approx V_{OL}$	linear	sat^n.
E	$> (V_{DD}+V_{TO,p})$	V_{OL}	linear	cut off.

Region A :-

In this region $V_{in} < V_{TO,n}$, the nMOS is cut off & the O/P voltage is equal to $V_{OH} = V_{DD}$.

When the i/p voltage is increased beyond $V_{TO,n}$, the nMOS transistor starts conducting in satn mode and the O/P voltage begins to decrease.

Region B :- The critical voltage V_{IL} corresponds to $\frac{dV_{out}}{dV_{in}} = -1$. is placed within the region B.

Region C :-

As the O/P voltage further decreases, the pMOS transistor enters satn at the boundary of Region C. From fig, the inverter threshold voltage where $V_{in} = V_{out}$ is placed in region C.

Region D :-

At the time the O/P voltage V_{out} falls below $V_{in} - V_{TO,p}$ the nMOS starts to operates in linear mode. This happens in region D where the critical voltage point V_{IH} with $\frac{dV_{out}}{dV_{in}} = -1$ is placed.

Region E:-

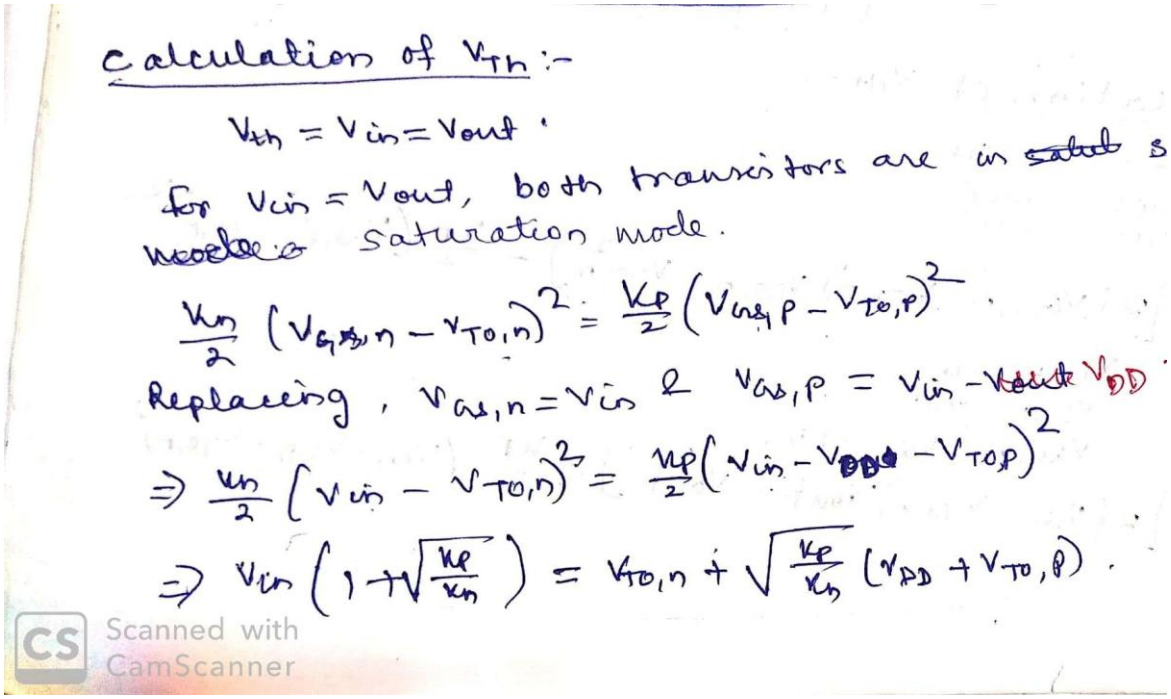
In this region, $V_{in} > V_{DD} + V_{TO,P}$, the PMOS transistor is cut off and the o/p voltage is.

$V_{OL} = 0$;-

$$\boxed{\begin{matrix} V_{OH} = V_{DD} \\ V_{OL} = 0 \end{matrix}}$$ for CMOS inverter

Q-6. Find the expression for threshold voltage for CMOS inverter.

Ans:



Calculation of V_{Th} :-

$V_{th} = V_{in} = V_{out}$.

for $V_{in} = V_{out}$, both transistors are in saturation mode.

$$\frac{K_n}{2}(V_{GS,n} - V_{TO,n})^2 = \frac{K_p}{2}(V_{GS,P} - V_{TO,P})^2$$

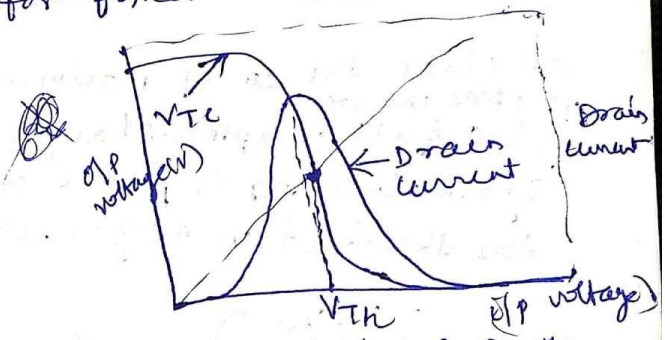
Replacing, $V_{GS,n} = V_{in}$ & $V_{GS,P} = V_{in} - V_{DD}$

$$\Rightarrow \frac{K_n}{2}(V_{in} - V_{TO,n})^2 = \frac{K_p}{2}(V_{in} - V_{DD} - V_{TO,P})^2$$

$$\Rightarrow V_{in}\left(1 + \sqrt{\frac{K_p}{K_n}}\right) = V_{TO,n} + \sqrt{\frac{K_p}{K_n}}(V_{DD} + V_{TO,P})$$

$$\therefore V_{Th} = \frac{V_{TO,n} + \sqrt{\frac{K_p}{K_n}}(V_{DD} + V_{TO,P})}{\left(1 + \sqrt{\frac{K_p}{K_n}}\right)} \quad \text{---} (2)$$

The threshold voltage V_{th} is a function of the transconductance ratio K_R, for fixed values of V_{DD}, $V_{TO,n}$ & $V_{TO,P}$.



Typical V_{TC} & power supply current of CMOS inverter ckt

Q-7. Design the CMOS inverter taking all the parameters .

Ans:

Design of CMOS inverter:-

→ The CMOS inverter gives a full swing of o/p voltage between 0 to V_{DD} due to the complementary push pull op.

→ So it has relatively wide noise margins.

→ Rearranging eq^n (2) we get:-

(K_R) → design Parameter

$$\Rightarrow V_{Th}\left(1 + \sqrt{1/K_R}\right) = V_{TO,n} + \sqrt{1/K_R}\,(V_{DD} + V_{TO,P})$$

$$\Rightarrow V_{Th} + V_{Th}\sqrt{1/K_R} = V_{TO,n} + \sqrt{1/K_R}\,V_{DD} + \sqrt{1/K_R}\,V_{TO,P}$$

$$\Rightarrow \sqrt{\frac{1}{K_R}}\,(V_{Th} - V_{DD} - V_{TO,P}) = V_{TO,n} - V_{Th}$$

$$\Rightarrow \sqrt{\frac{1}{K_R}} = \frac{V_{TO,n} - V_{Th}}{V_{Th} - V_{DD} + V_{TO,P}} = \frac{V_{Th} - V_{TO,n}}{V_{DD} + V_{TO,P} - V_{Th}}$$

$$\Rightarrow K_R = \left(\frac{V_{DD} + V_{TO,P} - V_{Th}}{V_{th} - V_{TO,n}}\right)^2 = \frac{K_n}{K_P}$$

We know $V_{th(ideal)} = \frac{V_{DD}}{2}$.

$\therefore \left(\frac{K_n}{K_p}\right)_{ideal} = \left(\frac{0.5V_{DD} + V_{TO,P}}{0.5V_{DD} - V_{TO,n}}\right)^2$

Q.8. Find the critical voltages of a symmetric CMOS inverter and write the condition for symmetric inverter.

Ans:

CMOS Symmetric Inverter

Since the operations of nMOS and pMOS transistors of CMOS inverter are full complementary to each other, we can achieve symmetric i/p input & o/p characteristics by scaling the threshold voltages as $V_{TO} = V_{TO,n} = |V_{TO,P}|$ Cond'n ①

$\left(\frac{K_n}{K_p}\right)_{\text{symmetric inverter}} = 1$. (Cond'n ②)

The ratio K_R is defined as

$\frac{K_n}{K_p} = \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}{\mu_p C_{ox}\left(\frac{W}{L}\right)_p} = \frac{\mu_n\left(\frac{W}{L}\right)_n}{\mu_p\left(\frac{W}{L}\right)_P} = 1$

$\Rightarrow \frac{(W/L)_n}{(W/L)_P} = \frac{\mu_P}{\mu_n} \approx \frac{230\ cm^2/V.s}{580\ cm^2/V.s}$

$\Rightarrow \boxed{\left(\frac{W}{L}\right)_P \cong 2.5\left(\frac{W}{L}\right)_n}$ ✓

For symmetric CMOS inverter, with $V_{TO,n} = |V_{TO,P}|$ & $K_R = 1$, the critical voltage V_{IL}

$V_{IL} = \frac{2V_{out} + V_{TO,P} - V_{DD} + K_R V_{TO,n}}{(1 + K_R)}$

$= \frac{2V_{out} + V_{TO,n} - V_{DD} + V_{TO,n}}{2}$

$= \frac{2V_{out} + 2V_{TO,n} - V_{DD}}{2}$.

Applying KCL,

$$\frac{K_n}{2}(V_{in}-V_{TO,n})^2 = \frac{K_p}{2}\left[2(V_{in}-V_{DD}-V_{TO,P})(V_{out}-V_{DD})-(V_{out}-V_{DD})^2\right]$$

Substituting $\frac{K_n}{K_P} = K_R = 1$.

$$(V_{in}-V_{TO,n})^2 = \left[2(V_{in}-V_{DD}-V_{TO,P})(V_{out}-V_{DD})-(V_{out}-V_{DD})^2\right]$$

Putting $V_{in} = V_{IL}$ and solving we get.

$$\boxed{V_{IL} = \frac{1}{8}(3V_{DD}+2V_{TO,n})}$$

Also the critical voltage V_{IH} is found as

$$\boxed{V_{IH} = \frac{1}{8}(5V_{DD}-2V_{TO,n})}$$

For a symmetric inverter :-

$$\boxed{V_{IL}+V_{IH} = V_{DD}}$$

The noise margins NM_L & NM_H for this symmetric CMOS inverter are now calculated as.

$$NM_L = V_{IL} - V_{OL} = V_{IL}$$

$$NM_H = V_{OH} - V_{IH} = V_{DD} - V_{IH}$$

$$= V_{IL} + V_{IH} - V_{IH}$$

$$= V_{IL} = NML = NMH$$

$$\therefore \boxed{NM_L = NM_H = V_{IL}}$$

$$K_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

$$K_p = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$$

Power $\left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$.

Q.9. Consider the CMOS inverter :

V_{DD}=3.3V

$V_{TO,n}$=0.6V

$V_{TO,p}$=- 0.7V

k_n=200 µA/V^2

k_p=80 µA/V^2

Calculate the noise margin of the circuit with k_R=2.5, $V_{TO,n} \neq V_{TO,p}$, not symmetric.

Soln:-

$$V_{IL} = \frac{2V_{out} + V_{TO,p} - V_{DD} + k_R V_{TO,n}}{1+k_R}$$

$$= \frac{2V_{out} - 0.7 - 3.3 + 2.5 \times 0.6}{3.5}$$

$$= 0.57 V_{out} - 0.71.$$

Now substitute this expr^n into KCL.

$$\frac{k_n}{2}(V_{in} - V_{TO,n})^2 = \frac{k_p}{2}\left[2(V_{in} - V_{DD} - V_{TO,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

$$\Rightarrow k_R (V_{in} - V_{TO,n})^2 = \left[2(V_{in} - V_{DD} - V_{TO,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2\right]$$

$$\Rightarrow 2.5 (0.57 V_{out} - 0.71 - 0.6)^2 = \left[2(0.57 V_{out} - 0.71 - 3.3 + 0.7)(V_{out} - 3.3) - (V_{out} - 3.3)^2\right]$$

$$\Rightarrow 2.5(0.57 V_{out} - 1.31)^2 = \left[2(0.57 V_{out} - 3.31)(V_{out} - 3.3) - (V_{out} - 3.3)^2\right]$$

$$\Rightarrow 2.5(0.57^2 V_{out}^2 + 1.31^2 - 2 \times 0.57 V_{out} \times 1.31)$$

$$= 2(0.57 V_{out}^2 - 1.88 V_{out} - 3.31 V_{out} + 10.95] - V_{out}^2 - 10.89 + 6.6 V_{out}]$$

$$\Rightarrow 0.66 V_{out}^2 - 0.05 V_{out} - 6.65 = 0.$$

for $V_{out} > 0$. only one root is considered.

$$V_{out} = 3.14 V$$

So, $V_{IL} = 0.57 \times 3.14 - 0.71 = 1.08 V$.

$$V_{IH} = \frac{V_{DD} + V_{TO,p} + k_R (2V_{out} + V_{TO,n})}{1 + k_R}$$

$$= 1.43 V_{out} + 1.17$$

By KCL, we get $V_{out} = 0.27 V$

$$V_{IH} = 1.43 \times 0.27 + 1.17 = 1.55 V.$$

$$NM_L = V_{IL} - V_{OL} = 1.08 V$$

$$NM_H = V_{OH} - V_{IH} = 1.75 V.$$

Q.10. Calculate the noise margin of a CMOS inverter with V_{DD}=5V, $V_{TO,n}$=1V, $V_{TO,p}$=-1V.k_n=k_p=200 µA/V^2

Soln:-

$V_{TO,n} = |V_{TO,P}| = 1V$

$K_n = K_p = 200\ \mu A/V^2$

So, the inverter is symmetric.

$\therefore NM_L = NM_H = V_{IL}$.

$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_{TO,n})$$

$$= \frac{1}{8}(3\times 5 + 2\times 1)$$

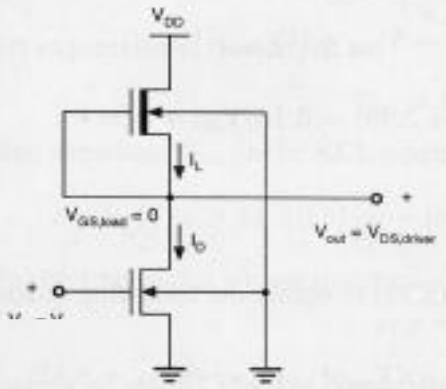
$$= 17/8\ V. = 2.125V.$$

$\therefore NM_L = NM_H = V_{IL} = \underline{2.125V}$ Ans

The closed form delay expr^n will be derived under the assumption of pure excitation for lumped load capacitances. While exact SPICE circuit simulations (SPICE) usually provides accurate estimation of time domain behaviour of complex circuits.

Q-11.

Calculate the critical voltages (V_{OL}, V_{OH}, V_{IL}, V_{IH}) and find the noise margins of the following depletion-load inverter circuit:



$V_{DD} = 5$ V
$V_{T0,driver} = 1.0$ V
$V_{T0,load} = -3.0$ V
$(W/L)_{driver} = 2$, $(W/L)_{load} = 1/3$
$k_{n,driver}' = k_{n,load}' = 25\ \mu A/V^2$
$\gamma = 0.4\ V^{1/2}$
$\phi_F = -0.3$ V

First, the output high voltage is simply found according to (5.36) as $V_{OH} = V_{DD} = 5$ V.

To calculate the output low voltage V_{OL}, we must solve (5.33) and (5.38) simultaneously, using numerical iterations. We start the iterations by assuming that the output voltage is equal to zero, thus letting $V_{T,load} = V_{T0,load} = -3$ V. Solving (5.38) with this assumption yields a first-order estimate for V_{OL}.

$$V_{OL} = V_{OH} - V_{T0} - \sqrt{(V_{OH} - V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right) \cdot |V_{T,load}(V_{OL})|^2}$$

$$= 5 - 1 - \sqrt{(5-1)^2 - \left(\frac{1}{6}\right)|3|^2} = 0.192 \text{ V}$$

Now, the threshold voltage of the depletion-load device can be updated by substituting this output voltage into (5.33).

$$V_{T,load} = V_{T0,load} + \gamma\left(\sqrt{|2\phi_F| + V_{OL}} - \sqrt{|2\phi_F|}\right)$$

$$= -3 + 0.4\left(\sqrt{0.6 + 0.2} - \sqrt{0.6}\right) = -2.95 \text{ V}$$

Using this new value for $V_{T,load}$, we now recalculate V_{OL}, again according to (5.38).

$$V_{OL} = 0.186 \text{ V}$$

$$V_{T,load} = -2.95 \text{ V}$$

MOS INVERTERS

SWITCHING CHARACTERISTICS AND INTERCONNECT EFFECTS

MULTIPLE CHOICE QUESTIONS

1. Rise time and fall time is _____ to load capacitance C_L
a) directly proportional
b) inversely proportional
c) exponentially equal
d) not related

2. Rise time and fall time is _____ to Vdd
a) directly proportional
b) inversely proportional
c) exponentially equal
d) not related

3. Propagation time is directly proportional to
a) x
b) 1/x
c) x^2
d) $1/x^2$

4. Total capacitance can be given as
a) n(square Cg)
b) nc(square Cg)
c) c(square Cg)
d) square Cg

5. Overall delay is directly proportional to
a) n
b) 1/n
c) n^2
d) $1/n^2$

6. Buffer is used because
a) it increases the speed
b) decreases sensitivity to noise
c) decreases speed
d) does not affect speed

7. The overall delay is _____ to the relative resistance r
a) directly proportional
b) inversely proportional
c) exponentially proportional
d) not dependent

8. Overall delay increases as n
a) increases
b) decreases
c) exponentially decreases
d) logarithmically decreases

9. Increasing fan-out, _____ the propagation delay
a) increases
b) decreases
c) does not affect
d) exponentially decreases

10. Inverter with matched transistor will have
   a) high τ_{PHL}
   b) high τ_{PLH}
   c) low τ_{PLH}
   d) equal τ_{PLH} and τ_{PHL}

11. K_n=
   a) kn'$(W/L)_n$
   b) kp'$(W/L)_p$
   c) kn'$(W/L)_p$
   d) kp'$(W/L)_n$

12. Dynamic power dissipation of high density chips are in range of
   a) ones of watts
   b) tens of watts
   c) hundreds of watts
   d) thousands of watts

Answer key: 1(a),2(b),3(c),4(b),5(c),6(a), 7(a), 8(a), 9(a),10(d), 11(a), 12(b)

SUBJECTIVE QUESTIONS:

1. Consider the CMOS inverter circuit, with VDD=3.3V. The I-V characteristics of then MOS transistor are specified as follows: When V_{GS}=3.3V, the drain current reaches its saturation level Isat=2mA forVDS≥2.5V.Assume that the input signal applied to the gate is a step pulse that switches instantaneously from 0V to 3.3V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 3.3 V to 1.65V, assuming an output load capacitance of 300fF.

Solution:

For the solution, consider the simplified pull-down circuit shown in Fig.5.We will assume that then MOS transistor operates in saturation from t=0 to t=t1'=t_{sat} and that it will operate in the linear region from t=t1'=t_{sat} to t=t2=t_{delay}. We can also deduce from the I-V characteristics that $V_{T,n}$=0.8V,since then MOS transistor enter saturation when $V_{DS}>V_{GS}-V_{T,n}$.

The voltage V_{GS} is equal to 3.3V for t≥0.

•The current equation for the saturation region can be written as

$$C\frac{dV_{out}}{dt} = -I_D = -I_{sat} = -\frac{1}{2}k_n\left(V_{OH} - V_{T,n}\right)^2$$

•We can calculate the amount of time in which the nMOS transistor operates in saturation (tsat), by integrating this equation.

$$\int_{t=0}^{t=t_{sat}} dt = -\int_{V_{out}=3.3}^{V_{out}=2.5} \frac{C}{I_D} dV_{out}$$

$$t_{sat} = \frac{V_{T,n}C}{I_{sat}} = \frac{0.8\,\text{V}\cdot 300\,\text{fF}}{2\,\text{mA}} = 120[\text{ps}]$$

The transconductance k_n of the nMOS transistor can be found as follows:

$$k_n = \frac{2I_{sat}}{\left(V_{OH} - V_{T,n}\right)^2} = \frac{2\times 2\times 10^{-3}}{(3.3-0.8)^2} = 0.640\times 10^{-3}\left[\text{A}/\text{V}^2\right]$$

Now, the current equation for the linear operating region is

$$C\frac{dV_{out}}{dt} = -I_D = -\frac{1}{2}k_n\left[2\left(V_{OH} - V_{T,n}\right)V_{out} - {V_{out}}^2\right]$$

Integrating this differential equation between the two voltage boundary conditions yields the time in which the nMOS transistor operates in the linear region during this transition.

$$\int_{t=t_{sat}}^{t=t_{delay}} dt = -2C \int_{V_{out}=2.5}^{V_{out}=1.65} \frac{dV_{out}}{k_n\left[2\left(V_{OH}-V_{T,n}\right)V_{out}-V_{out}^{\,2}\right]}$$

$$t_{delay}-t_{sat} = -\frac{C}{k_n}\frac{1}{\left(V_{OH}-V_{T,n}\right)}\ln\left(\frac{V_{out}}{2\left(V_{OH}-V_{T,n}\right)-V_{out}}\right)\Bigg|_{V_{out}=2.5}^{V_{out}=1.65}$$

$$= \frac{C}{k_n}\frac{1}{\left(V_{OH}-V_{T,n}\right)}\left[\ln\left(\frac{2\left(V_{OH}-V_{T,n}\right)-V_{1.65}}{V_{1.65}}\right)-\ln\left(\frac{2\left(V_{OH}-V_{T,n}\right)-V_{2.5}}{V_{2.5}}\right)\right]$$

$$= \frac{0.3\times10^{-12}}{0.640\times10^{-3}}\frac{1}{(3.3-0.8)}\left[\ln\left(\frac{5-1.65}{1.65}\right)-\ln\left(\frac{5-2.5}{2.5}\right)\right]=133[\text{ps}]$$

Thus, the total delay time is found to be

$$t_{delay}=120+133=253[\text{ps}]$$ (Ans)

2. For the CMOS inverter shown in Fig.1 with a power supply voltage of V_{DD}=5V, determine the fall time τ_{fall} which is defined as the time elapsed between the time point at which $V_{out}=V_{90\%}$=4.5V and the time point at which $V_{out}=V_{10\%}$=0.5V. Use both the average-current method and the differential equation method for calculating τ_{fall}. The output load capacitance is 1 pF.

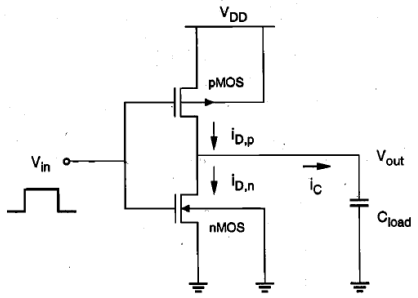


Fig.1. CMOS inverter

The nMOS transistor parameters are given as

$\mu_n C_{ox}$ = 20 μA/V²
$(W/L)_n$ = 10
$V_{T,n}$ = 1.0 V

Solution :

Using a simple expression similar to (Eqn.10),we can determine the average capacitor current during the charge-down event described above

$$I_{avg} = \frac{1}{2}\left[I(V_{in} = 5\ \text{V}, V_{out} = 4.5\ \text{V}) + I(V_{in} = 5\ \text{V}, V_{out} = 0.5\ \text{V})\right]$$
$$= \frac{1}{2}\left[\frac{1}{2}k_n\left(V_{in} - V_{T,n}\right)^2 + \frac{1}{2}k_n\left(2\left(V_{in} - V_{T,n}\right)V_{out} - {V_{out}}^2\right)\right]$$
$$= \frac{1}{2}\cdot\frac{1}{2}\cdot 20\times10^{-6}\cdot 10\left[(5-1)^2 + \left(2(5-1)0.5 - 0.5^2\right)\right] = 0.9875\ [\text{mA}]$$

The fall time is then found as

$$\tau_{fall} = \frac{C\cdot\Delta V}{I_{avg}} = \frac{1\times10^{-12}(4.5-0.5)}{0.9875\times10^{-3}} = 4.05\times10^{-9}\ [\text{s}] = 4.05\ [\text{ns}]$$

Now, we will recalculate the fall time using the differential equation approach. Then MOS transistor operates in the saturation region for 4.0V<Vout<4.5V. Writing the current equation for the saturation region, we obtain

$$C\frac{dV_{out}}{dt} = -\frac{1}{2}k_n\left(V_{in} - V_{T,n}\right)^2, \text{ where } \quad k_n = \mu_n C_{ox}\left(\frac{W}{L}\right)_n$$

$$\frac{dV_{out}}{dt} = \frac{-20\times10^{-6}\cdot10\cdot(5-1)^2}{2\cdot1\times10^{-12}} = -1.6\times10^{9}\ [\text{V/s}]$$

Integrating this simple expression yields the time during which the nMOS transistor operates in saturation

$$\int_{t=0}^{t=t_{sat}} dt = -\frac{1}{1.6\times10^{9}}\int_{V_{out}=4.5}^{V_{out}=4} dV_{out}$$

$$t_{sat} = \frac{0.5}{1.6\times10^{9}} = 0.3125\times10^{-9}\ [s] = 0.3125\ [ns]$$

Then MOS transistor operates in the linear region for 0.5V<V<4.0V.

The current equation for this operating region is written as follows:

$$C\frac{dV_{out}}{dt} = -\frac{1}{2}k_n\left[2\left(V_{in} - V_{T,n}\right)V_{out} - {V_{out}}^2\right]$$

Integrating this equation, we obtain the delay component during which the nMOS transistor operates in the linear region.

$$\int_{t=t_{sat}}^{t=t_{delay}} dt = -2C\int_{V_{out}=4}^{V_{out}=0.5} \frac{dV_{out}}{k_n\left[2\left(V_{in} - V_{T,n}\right)V_{out} - {V_{out}}^2\right]}$$

$$\tau_{fall} - t_{sat} = \frac{C}{k_n}\frac{1}{\left(V_{in} - V_{T,n}\right)}\left[\ln\left(\frac{2\left(V_{in} - V_{T,n}\right) - V_{0.5}}{V_{0.5}}\right) - \ln\left(\frac{2\left(V_{in} - V_{T,n}\right) - V_{4.0}}{V_{4.0}}\right)\right]$$

$$= \frac{1\times10^{-12}}{20\times10^{-6}\cdot10\cdot4}\left[\ln\left(\frac{8-0.5}{0.5}\right) - \ln\left(\frac{8-4}{4}\right)\right] = 3.385\times10^{-9}\ [\text{s}] = 3.385\ [\text{ns}]$$

Thus, the fall time of the CMOS inverter is found as follows:

$$\tau_{fall} = 3.6975\ [\text{ns}]$$

3. Design a CMOS inverter by determining the channel widths W_n and W_p of the nMOS and pMOS transistors, to meet the following performance specifications. V_{th}=1.5V for V_{DD}=3V, Propagation delay times τ^*_{PHL}<0.2ns and τ^*_{PLH}<0.15ns, A falling delay of 0.35ns for an output transition from 2V to 0.5V,assuming a combined output load capacitance of 300fF and ideal step input.

Solution:

First, the minimum (W/L) ratios of the nMOS and pMOS transistors which are dictated by the propagation delay constraints can be found as follows.

$$\left(\frac{W_n}{L_n}\right) = \frac{C_{load}}{\tau^*_{PHL}\,\mu_n\,C_{ox}\left(V_{DD} - V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD} - V_{T,n}} + \ln\left(\frac{4\left(V_{DD} - V_{T,n}\right)}{V_{DD}} - 1\right)\right]$$

$$= \frac{300\times10^{-15}}{0.2\times10^{-9}\cdot120\times10^{-6}\cdot(3-0.8)}\left[\frac{2\cdot0.8}{3-0.8} + \ln\left(\frac{4(3-0.8)}{3} - 1\right)\right] = 7.9$$

$$\left(\frac{W_p}{L_p}\right) = \frac{C_{load}}{\tau^*_{PLH}\,\mu_p\,C_{ox}\left(V_{DD} - \left|V_{T,p}\right|\right)}\left[\frac{2\left|V_{T,p}\right|}{V_{DD} - \left|V_{T,p}\right|} + \ln\left(\frac{4\left(V_{DD} - \left|V_{T,p}\right|\right)}{V_{DD}} - 1\right)\right]$$

$$= \frac{300\times10^{-15}}{0.15\times10^{-9}\cdot60\times10^{-6}\cdot(3-1)}\left[\frac{2\cdot1}{3-1} + \ln\left(\frac{4(3-1)}{3} - 1\right)\right] = 25.2$$

During the falling output transition (from 2 V to 0.5V) described above, the nMOS transistor of the CMOS inverter will operate entirely in the linear region. The current equation of the nMOS transistor in this region is

$$C_{load}\frac{dV_{out}}{dt}=-\frac{1}{2}\mu_n C_{ox}\frac{W_n}{L_n}\left[2\left(V_{OH}-V_{T0,n}\right)V_{out}-{V_{out}}^2\right]$$

Integrating the above equation

$$t_{delay}=0.35\times10^{-9}=-2C_{load}\int_{V_{out}=2}^{V_{out}=0.5}\frac{dV_{out}}{\mu_n C_{ox}\frac{W_n}{L_n}\left[2\left(V_{OH}-V_{T0,n}\right)V_{out}-{V_{out}}^2\right]}$$

$$t_{delay}=\frac{-C_{load}}{\mu_n C_{ox}\frac{W_n}{L_n}}\frac{1}{\left(V_{OH}-V_{T0,n}\right)}\ln\left(\frac{V_{out}}{2\left(V_{OH}-V_{T0,n}\right)-V_{out}}\right)\Bigg|_2^{0.5}$$

$$t_{delay}=\frac{-C_{load}}{\mu_n C_{ox}\left(\frac{W_n}{L_n}\right)}\frac{1}{(3-0.8)}\left[\ln\left(\frac{0.5}{2(3-0.8)-0.5}\right)-\ln\left(\frac{2}{2(3-0.8)-2}\right)\right]$$

$$0.35\times10^{-9}=\frac{-300\times10^{-15}}{120\times10^{-6}\left(\frac{W_n}{L_n}\right)2.2}\left[-2.054+0.182\right]$$

Let

$$\left(\frac{W_n}{L_n}\right)=6.1$$

Notice that this ratio is smaller than the(W/L)-ratio found from the propagation delay constraint.

•Thus, we take the larger ratio which will satisfy both timing constraints, and determine the size of then MOS transistor as W_n=4.7μm,for the given L_n=0.6μm.

Next, the logic threshold constraint of Vth=1.5V will help determine the pMOS transistor dimensions.

$$V_{th}=\frac{V_{T0,n}+\sqrt{\frac{1}{k_R}}\left(V_{DD}+V_{T0,p}\right)}{1+\sqrt{\frac{1}{k_R}}}=1.5$$

We find that the ratio k_R which satisfies this design constraint is equal to 0.51.

4. Write the expression for the total capacitive load of the inverter.

Solution: The total capacitive load of the inverter can now be expressed as

$$C_{load} = \alpha_0 + \alpha_n W_n + \alpha_p W_p$$

Where

$$\alpha_0 = 2 D_{drain} \left(C_{jsw,n} K_{eq,n} + C_{jsw,p} K_{eq,p} \right) + C_{int} + C_g$$

$$\alpha_n = K_{eq,n} \left(C_{j0,n} D_{drain} + 2 C_{jsw,n} \right)$$

$$\alpha_p = K_{eq,p} \left(C_{j0,p} D_{drain} + 2 C_{jsw,p} \right)$$

5. Describe the operation of CMOS Ring Oscillator.

Ans:

The cascade connection of three identical CMOS inverters are considered, as shown in Fig. 1, where the output node of the third inverter is connected to the input node of the first inverter. As such, the three inverters form a voltage feedback loop.

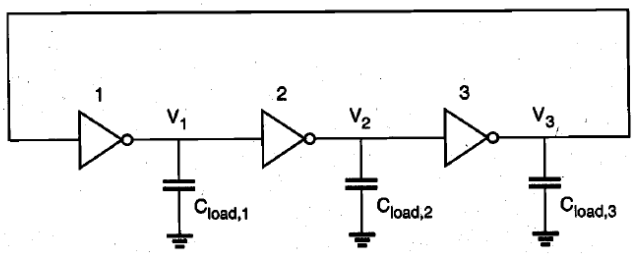


Fig.1. Three-stage ring oscillator circuit consisting of identical inverters.

In the three-stage circuit, the oscillation period T of any of the inverter output voltages can be expressed as the sum of six propagation delay times(Fig.2). Since the three inverters in the closed-loop cascade connection are assumed to be identical, and since the output load capacitances are equal to each other (Cload1=Cload2=Cload3); we can express the oscillation period T in terms of the average propagation delay τ_p, as

$$T = \tau_{PHL1} + \tau_{PLH1} + \tau_{PHL2} + \tau_{PLH2} + \tau_{PHL3} + \tau_{PLH3}$$
$$= 2\tau_P + 2\tau_P + 2\tau_P$$
$$= 3 \cdot 2\tau_P = 6\tau_P$$

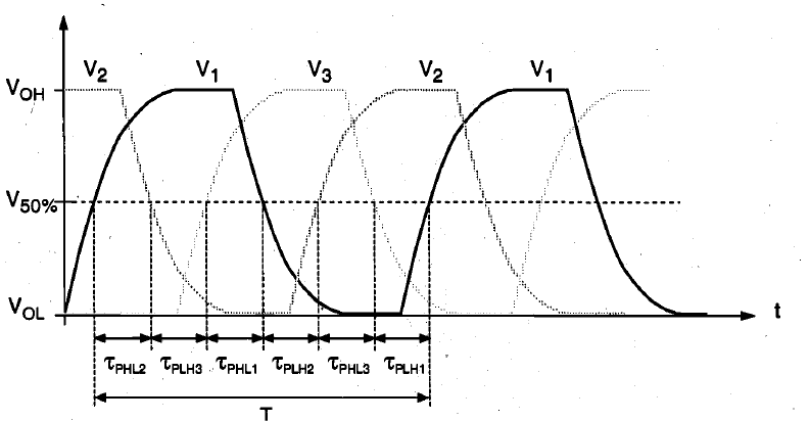


Fig.2. Typical voltage waveforms of the three inverters shown in Fig. 1.

Generalizing this relationship for an arbitrary odd number(*n*) of cascade-connected inverters, we obtain the oscillation frequency(*f*) is found to be a very simple function of the average propagation delay of an inverter stage.

$$f = \frac{1}{T} = \frac{1}{2 \cdot n \cdot \tau_P}$$

$$\tau_P = \frac{1}{2 \cdot n \cdot f}$$

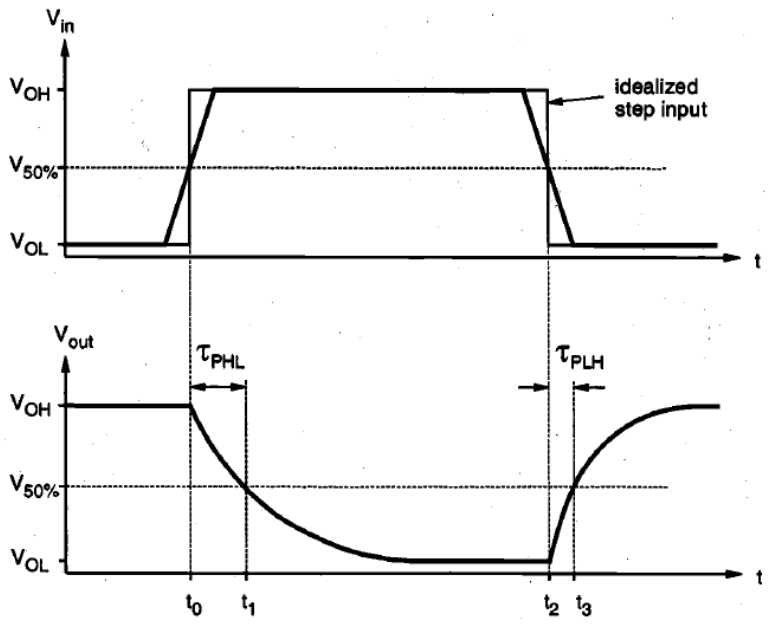
Typically, the number n is made much larger than just 3or 5,in order to keep the oscillation frequency of the circuit within an easily measurable range.

•The ring oscillator circuit can be used as a very simple pulse generator, where the output wave form is utilized as a simple master clock signal generated on-chip.

6. Define τ_{PHL} and τ_{PLH}

Ans: τ_{PHL} is the time delay between the $V_{50\%}$ - transition of the rising input voltage and the $V_{50\%}$ - transition of the falling output voltage.

τ_{PLH} is defined as the time delay between the V50%-transition of the falling input voltage and the V50%-transition of the rising output voltage



7. Write the expression for average propagation delay.

Ans: The average propagation delay τ_P of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

8. What is rise time and fall time?

Ans: The rise time τ_{rise} is defined here as the time required for the output voltage to rise from the $V_{10\%}$ level to $V_{90\%}$ level.

The fall time τ_{fall} is defined here as the time required for the output voltage to drop from the $V_{90\%}$ level to $V_{10\%}$ level.

The voltage levels $V_{10\%}$ and $V_{90\%}$ are defined as;

$$V_{10\%} = V_{OL} + 0.1 \cdot (V_{OH} - V_{OL})$$
$$V_{90\%} = V_{OL} + 0.9 \cdot (V_{OH} - V_{OL})$$

Thus, the output rise and fall times are found from Fig.1 as follows.

$$\tau_{fall} = t_B - t_A$$

$$\tau_{rise} = t_D - t_C$$

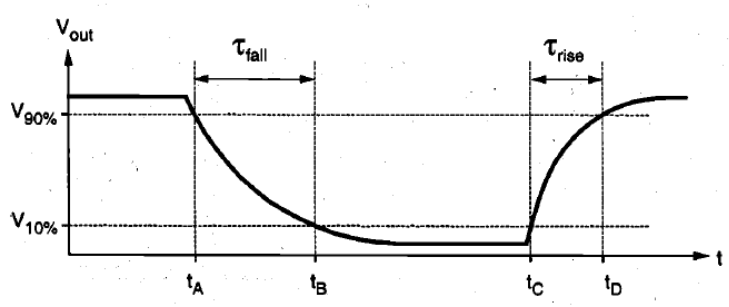


Fig.1. Output voltage rise and fall times.

9. What is power delay product? Briefly explain the use of PDP in CMOS Design.

Ans:

The power-delay product (PDP) is a fundamental parameter which is often used for measuring the quality and the performance of a CMOS process and gate design. As a physical quantity, the power-delay product can be interpreted as the average energy required for a gate to switch its output voltage from low to high and from high to low. We have already seen that in a CMOS logic gate, energy is dissipated

(i) by the pMOS network while the output load capacitance C_{load} is being charged up from 0 to VDD, and

(ii) by the nMOS network while the output load capacitance is being charged down from VDD to 0.

Following a simple analysis procedure which is very similar to the one used for deriving the average dynamic power dissipation in CMOS logic gates and ignoring the short-circuit and leakage currents, the amount of energy required to switch the output can be found as

$$PDP = C_{load} V_{DD}^2 \quad (1)$$

The energy described by (1) is mainly dissipated as heat when the nMOS and pMOS transistors conduct current during switching. Thus, from a design point-of-view, it is desirable to minimize the power-delay product. Since the PDP is a function of the output load capacitance and the power supply voltage, the designer should try to keep both C_{load} and VDD as small as possible when designing a CMOS logic gate. The power delay product is also defined as

$$PDP = 2 P^*_{avg} \tau_p \quad (2)$$

where P^*_{avg} is the average switching power dissipation at maximum operating frequency and τ_p is the average propagation delay. The factor of 2 in (2) accounts for *two* transitions of the output, from low to high and from high to low.

$$PDP = 2\left(C_{load}\, V_{DD}^{\,2}\, f_{max}\right)\tau_P$$
$$= 2\left[C_{load}\, V_{DD}^{\,2}\left(\frac{1}{\tau_{PHL}+\tau_{PLH}}\right)\right]\left(\frac{\tau_{PHL}+\tau_{PLH}}{2}\right)$$
$$= C_{load}\, V_{DD}^{\,2}$$

10. Explain the switching power dissipation of CMOS inverter.

ANS:

Consider the simple CMOS inverter circuit shown in Fig. 1. We will assume that the input voltage is an ideal step waveform with negligible rise and fall times. Typical input and output voltage waveforms and the expected load capacitor current waveform are shown in Fig. 2. When the input voltage switches from low to high, the pMOS transistor in the circuit is turned off, and the nMOS transistor starts conducting. During this phase, the output load capacitance $\mathbf{C_{load}}$ is being discharged through the nMOS transistor. Thus, the capacitor current equals the instantaneous drain current of the nMOS transistor. When the input voltage switches from high to low, the nMOS transistor in the circuit is turned off, and the pMOS transistor starts conducting. During this phase, the output load capacitance $\mathbf{C_{load}}$ is being charged up through the pMOS transistor; therefore, the capacitor current equals the instantaneous drain current of the pMOS transistor.

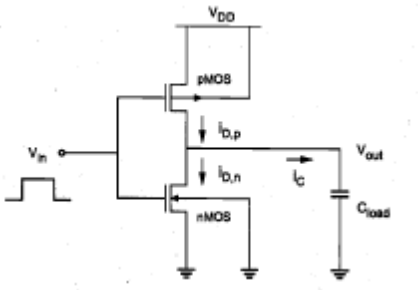


Fig.1: CMOS inverter used in dynamic power dissipation analysis

Assuming periodic input and output waveforms, the average power dissipated by any device over one period can be found as follows:

$$P_{avg} = \frac{1}{T}\int_0^T v(t).i(t)dt$$

Since during switching, the nMOS transistor and the pMOS transistor in a CMOS inverter conduct current for one-half period each, the average power dissipation of the CMOS inverter can be calculated as the power required to charge up and charge down the output load capacitance.

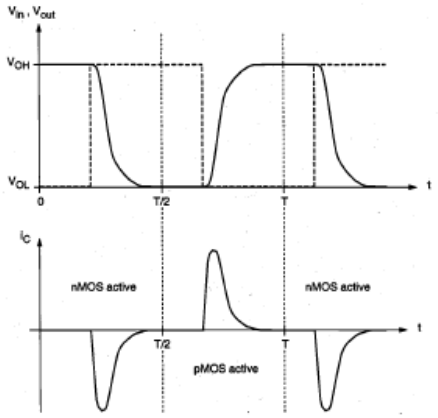


Fig:2. Typical input output characteristics during the dynamic power dissipation analysis of CMOS inverter

$$P_{avg} = \frac{1}{T}\left[\left(-C_{load}\frac{V_{out}^2}{2}\right)\Big|_0^{T/2} + \left(V_{DD}\cdot V_{out}\cdot C_{load} - \frac{1}{2}C_{load}V_{out}^2\right)\Big|_{T/2}^{T}\right]$$

$$P_{avg} = \frac{1}{T}C_{load}V_{DD}^2$$

Noting that $f = 1/T$, this expression can also be written as:

$$P_{avg} = C_{load}\cdot V_{DD}^2 \cdot f$$

It is clear that the average power dissipation of the CMOS inverter is proportional to the switching frequency i_f . Therefore, the low-power advantage of CMOS circuits becomes less prominent in high-speed operation, where the switching frequency is high. Also note that the average power dissipation is independent of all transistor characteristics and transistor sizes. Consequently, the switching delay times have no relevance to the amount of power consumption during the switching events. The reason for this is that the switching power is solely dissipated for charging and discharging the output capacitance from V_{OL} to V_{OH}, and vice versa.

11. Explain how the calculation of interconnect delay can be done using RC delay model and Elmore delay model.

ANS:

RC Delay Models

As we have already discussed in the previous Section, an interconnect line can be modeled as a lumped RC network if the time of flight across the interconnection line is significantly shorter than the signal rise/fall times. This is usually the case in most on-chip interconnects, thus, we will mainly concentrate on the calculation of delay in RC networks, in the following.

The simplest model which can be used to represent the resistive and capacitive parasitics of the interconnect line consists of one lumped resistance and one lumped capacitance (Fig1). Assuming that the capacitance is discharged initially, and assuming that the input signal is a rising step pulse at time t = 0, the output voltage waveform of this simple RC circuit is found as

$$V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{RC}}\right)$$

The rising output voltage reaches the 50%-point at $t = \tau_{plh}$, thus, we have

$$V_{50\%} = V_{DD}\left(1 - e^{-\frac{\tau_{PLH}}{RC}}\right)$$

and the propagation delay for the simple lumped RC network is found as

$$\tau_{PLH} \approx 0.69\,RC$$

This simple lumped RC network model provides a very rough approximation of the actual transient behavior of the interconnect line. The accuracy of the simple lumped RC model can be significantly improved by dividing the total line resistance into two equal parts (the T-model), as shown in Fig.2(a & b).

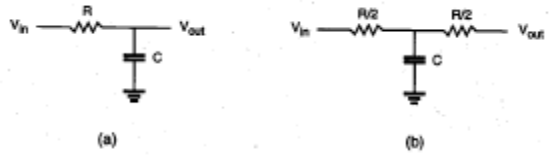


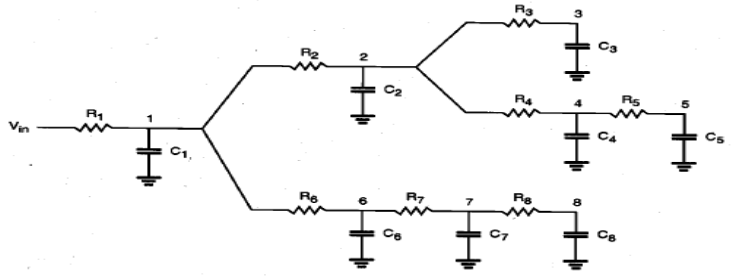
Fig.2(a)RC model (b) T model

The Elmore Delay

Consider a general RC tree network, as shown in Fig. below. Note that
(i) there are no resistor loops in this circuit,
(ii) all of the capacitors in an RC tree are connected between a node and the ground, and
(iii) there is one input node in the circuit. Also notice that there is a unique resistive path, from the input node to any other node in the circuit. Inspecting the general topology of this RC tree network, we can make the following path definitions:

* Let Pi denote the unique path from the input node to node i, i = 1, 2, 3, ..., N.

* Let $P_{ij} = P_i \cap P_j$ denote the portion of the path between the input and the node i, which is common to the path between the input and node j.



Assuming that the input signal is a step pulse at time $t = 0$, the Elmore delay at node i of

this RC tree is given by the following expression.

$$\tau_{Di} = \sum_{j=1}^{N} C_j \sum_{\substack{for\ all \\ k \in P_{ij}}} R_k$$

COMBINATIONAL MOS LOGIC CIRCUITS

MULTIPLE CHOICE QUESTIONS

1. When NMOS is turned ON in pseudo-NMOS logic, dynamic power is
   a) increased
   b) decreased
   c) infinite
   d) doesn't change
2. Pseudo-NMOS inverter, NMOS will be in triode region when
   A. $V_{input} \leq V_{th}$
   B. $v_{out} \geq V_{input} - V_{th}$
   C. $V_{out} < V_{input} - V_{th}$
   D. $v_{output} = V_{th}$

3. Topology of basic depletion-load inverter is identical to
   a) enhancement-load inverter
   b) depletion-load amplifier
   c) enhancement-load amplifier
   d) depletion-mode resistor
4. The output voltage of the CMOS NOR2 gate will attain

a) logic low level
b) logic high level
c)high impedance state
d) V_{th}

5. In CMOS TG

a) nMOS and pMOS are connected in series
b) nMOS and pMOS are connected in parallel
c) $V_{DD=}V_{th}$
d) none

6. In which network only nMOS pass transistors are used?

a) Pseudo nMOS
b) pass transistor gate
c) complex logic circuits
d) CPL logic

7. In CMOS 2 input NAND gate the switching threshold voltage $V_{th==} V_{DD}/2$ when

a) $k_n=k_p$
b) $k_n=4k_p$

c) $k_n=k_p/2$
d) $k_n=2k_p$

8) The value of V_{OH} for depletion load NOR2 gate is equal to
a) $V_{DD}/2$
b) V_{DD}
c) $2V_{DD}$
d) 0
9) In CPL circuits the inputs are
a) complementary to each other
b) same to each other
c) opposite to each other
d) none
10. The average power dissipation of the CMOS inverter is proportional to
a) V_{DD}
b) C_{load}
c) switching frequency, f
d) V_{OH}

ANSWER KEY: 1(b), 2(c), 3(b), 4(a),5(b), 6(d),7(b), 8(b),9(a), 10(c)

SUBJECTIVE QUESTIONS

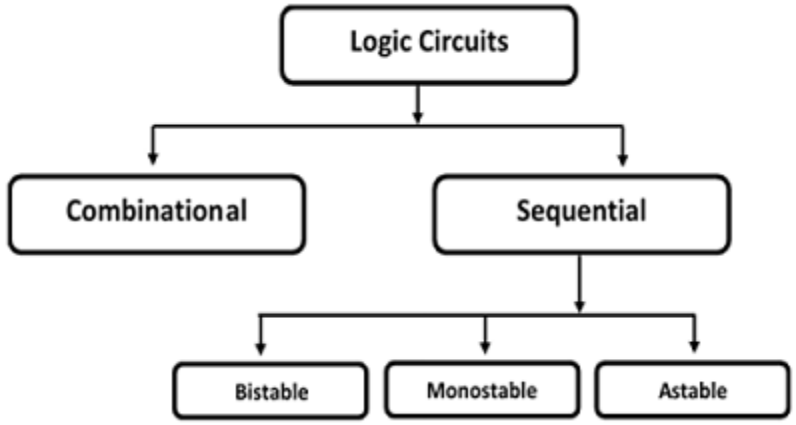
1. State the types of logic circuits in digital circuit design.

Ans.

Logic circuits are divided into two categories − (a) Combinational Circuits, and (b) Sequential Circuits.

In Combinational circuits, the output depends only on the condition of the latest inputs.

In Sequential circuits, the output depends not only on the latest inputs, but also on the condition of earlier inputs. Sequential circuits contain memory elements.



Sequential circuits are of three types −

Bistable − Bistable circuits have two stable operating points and will be in either of the states. Example − Memory cells, latches, flip-flops and registers.

Monostable − Monostable circuits have only one stable operating point and even if they are temporarily perturbed to the opposite state, they will return in time to their stable operating point. Example: Timers, pulse generators.

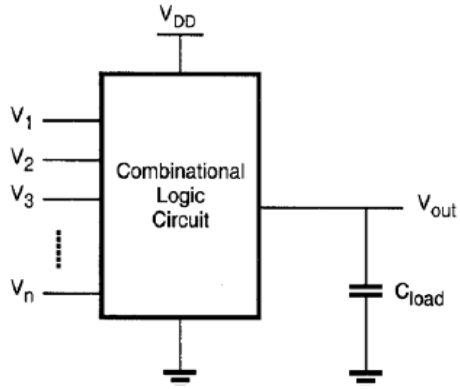
Astable − circuits have no stable operating point and oscillate between several states. Example − Ring oscillator.

2. What is combination logic design and what are its advantages?

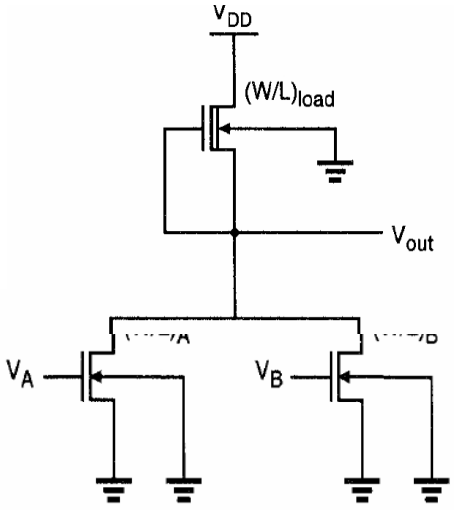
Ans:

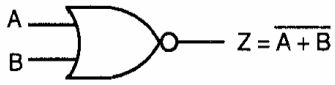
- Combinational logic circuits, or gates, which perform Boolean operations on multiple input variables and determine the outputs as Boolean functions of the inputs, are the basic building blocks of all digital systems.
- As shown in the figure below, all input variables are represented by node voltages, referenced to the ground potential. Using positive logic convention, the Boolean (or logic) value of " 1 " can be represented by a high voltage of VDD, and the Boolean (or logic) value of "0" can be represented by a low voltage of 0. The output node is loaded

with a capacitance CL, which represents the combined parasitic device capacitances in the circuit and the interconnect capacitance components seen by the output node. This output load capacitance certainly plays a very significant role in the dynamic operation of the logic gate.



3. Explain the operation and find V_{OH} and V_{OL} of depletion load 2 –input NOR gate.





V_A	V_B	V_{out}
low	high	low
high	low	low
high	high	lower

Calculation of V_{OH}, V_{OL}

Calculation of V_{OH}

When V_A and V_B are lower than threshold voltage ⇒ both off

$$I_{D,load}=\frac{k_{n,load}}{2}\cdot\left[2\left|V_{T,load}(V_{OH})\right|\cdot(V_{DD}-V_{OH})-(V_{DD}-V_{OH})^2\right]=0 \text{ than } \boxed{V_{OH}=V_{DD}}$$

Calculation of V_{OL}

Three case : (i)$V_A = V_{OH}$ $V_B = V_{OL}$ (ii)$V_A = V_{OL}$ $V_B = V_{OH}$ (iii)$V_A = V_{OH}$ $V_B = V_{OH}$

For the first two case : in case (i) $k_R=\frac{k_{driver,A}}{k_{load}}=\frac{k'_{n,driver}\left(\frac{W}{L}\right)_A}{k'_{n,load}\left(\frac{W}{L}\right)_{load}}$ in case (ii) $k_R=\frac{k_{driver,B}}{k_{load}}=\frac{k'_{n,driver}\left(\frac{W}{L}\right)_B}{k'_{n,load}\left(\frac{W}{L}\right)_{load}}$

$$\boxed{V_{OL}=V_{OH}-V_{T0}-\sqrt{(V_{OH}-V_{T0})^2-\left(\frac{k_{load}}{k_{driver}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}}$$

If the (W/L) ratios of both drivers are identical, the two V_{OL} will identical. In case (iii) both transistors are turned on, the saturated load current is the sum of the two linear - mode driver currents

$$I_{D,load}=I_{D,driverA}+I_{D,driverB}\Rightarrow\frac{k_{load}}{2}\left|V_{T,load}(V_{OL})\right|2=\frac{k_{driver,A}}{2}\left[2(V_A-V_{T0})V_{OL}-V_{OL}^2\right]+\frac{k_{driver,B}}{2}\left[2(V_B-V_{T0})V_{OL}-V_{OL}^2\right]$$

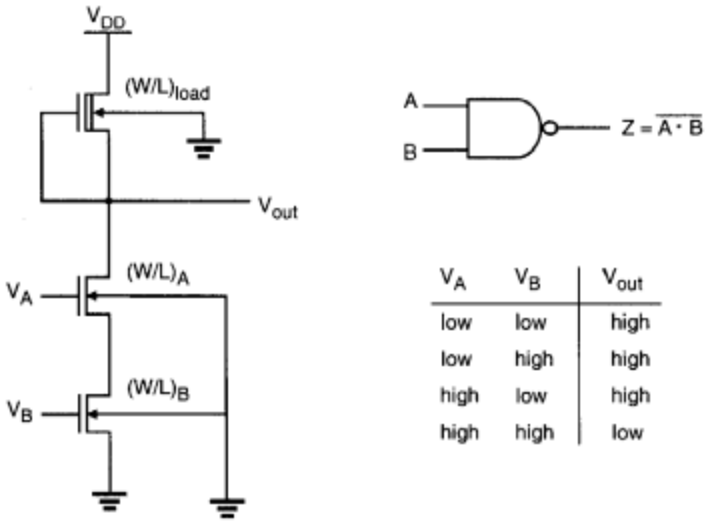
Since the gate voltages of both driver transistors are equal, we can devise an equivalent driver - to - load ratio for the NOR structure

$$k_R=\frac{k_{driver,A}+k_{driver,B}}{k_{load}}=\frac{k'_{n,driver}\left[\left(\frac{W}{L}\right)_A+\left(\frac{W}{L}\right)_B\right]}{k'_{n,load}\left(\frac{W}{L}\right)_{load}}\quad V_{OL}=V_{OH}-V_{T0}-\sqrt{(V_{OH}-V_{T0})^2-\left(\frac{k_{load}}{k_{driver,A}+k_{driver,B}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}$$

We usually set $k_{driver,A}=k_{driver,B}=k_Rk_{load}$

3. Explain the operation and find V_{OH} and V_{OL} of depletion load 2 –input NAND gate.

ANS:



V_A	V_B	V_{out}
low	low	high
low	high	high
high	low	high
high	high	low

Figure 1 A two-input depletion-load NAND gate, its logic symbol, and the corresponding truth table. Notice the substrate-bias effect for all nMOS transistors except one.

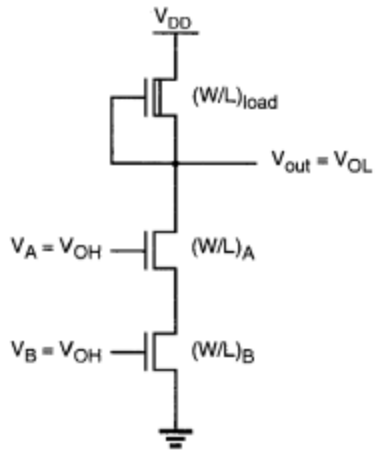


Figure The NAND2 gate with both of its inputs at logic-high level.

Calculation of V_{OH}, V_{OL}

When both input equal to $V_{OH} \Rightarrow I_{D,load} = I_{D,driverA} = I_{D,driverB}$

$$\frac{k_{load}}{2}\left|V_{T,load}(V_{OL})\right|^2 = \frac{k_{driver,A}}{2}\left[2(V_{GS,A}-V_{T,A})V_{DS,A}-V_{DS,A}^2\right] = \frac{k_{driver,B}}{2}\left[2(V_{GS,B}-V_{T,B})V_{DS,B}-V_{DS,B}^2\right]$$

Assume $V_{T,A} = V_{T,B} = V_{T0}$

$$V_{DS,A} = V_{OH} - V_{T0} - \sqrt{(V_{OH}-V_{T0})^2 - \left(\frac{k_{load}}{k_{driver,A}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}$$

$$V_{DS,B} = V_{OH} - V_{T0} - \sqrt{(V_{OH}-V_{T0})^2 - \left(\frac{k_{load}}{k_{driver,B}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}$$

$$V_{OL} \approx 2\left(V_{OH} - V_{T0} - \sqrt{(V_{OH}-V_{T0})^2 - \left(\frac{k_{load}}{k_{driver}}\right)\cdot\left|V_{T,load}(V_{OL})\right|^2}\right)$$

$$I_{D,A} = \frac{k_{driver}}{2}\left[2(V_{GS,A}-V_{T0})V_{DS,A}-V_{DS,A}^2\right] \quad I_{D,A} = \frac{k_{driver}}{2}\left[2(V_{GS,B}-V_{T0})V_{DS,B}-V_{DS,B}^2\right]$$

$$I_D = I_{D,A} = I_{D,B} = \frac{I_{D,A}+I_{D,B}}{2}$$

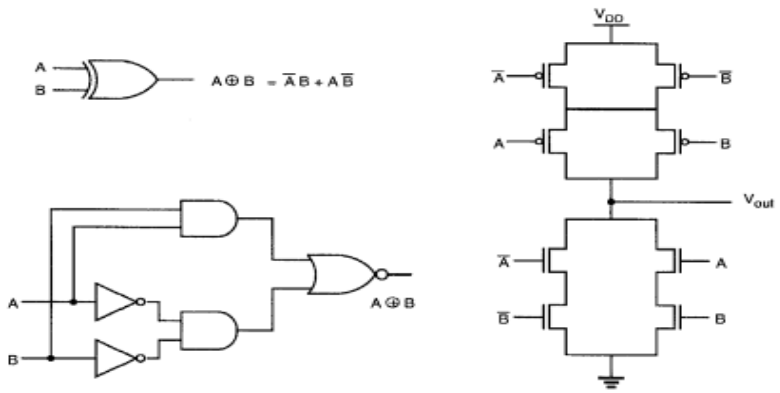
$$I_D = \frac{k_{driver}}{4}\left[2(V_{GS,B}-V_{T0})(V_{DS,A}+V_{DS,B})-(V_{DS,A}+V_{DS,B})^2\right]$$

$$I_D = \frac{k_{driver}}{4}\left[2(V_{GS}-V_{T0})V_{DS}-V_{DS}^2\right]$$

Two nMOS transistors connected in series and with the same gate voltage behave like *one* nMOS transistor with $k_{eq} = 0.5k_{driver}$

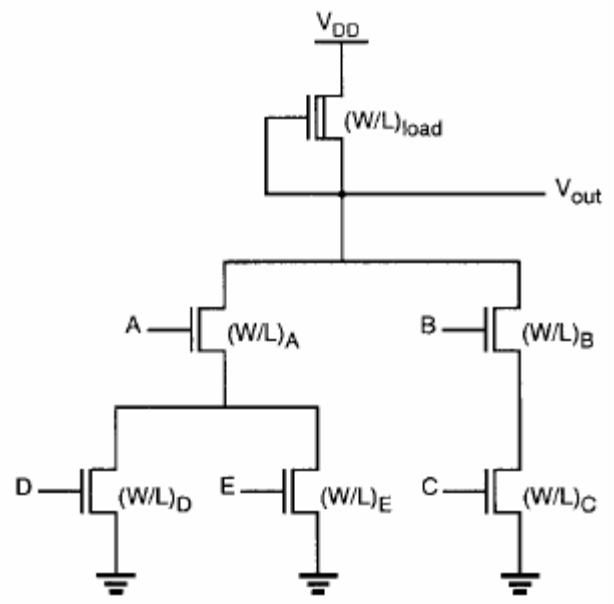
4. Design a CMOS implementation of XOR gate.

ANS:



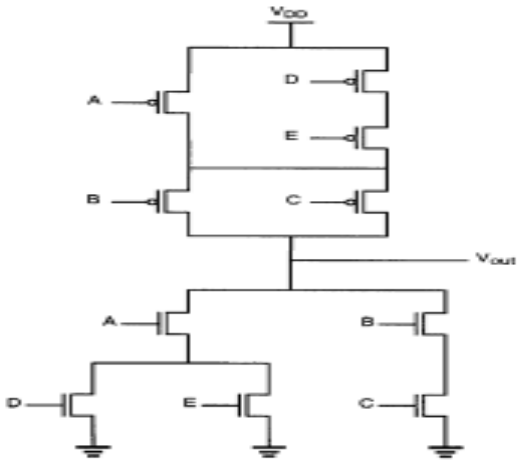
5. Design the nMOS implementation of complex logic function $Z=\overline{A(D+E)+BC}$ and find the $(W/L)_{equivalent}$ of the function. Draw the stick diagram implementation of the function Z using Euler path approach.

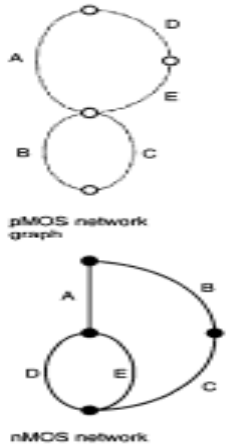
ANS:



$$\left(\frac{W}{L}\right)_{equivalent}=\frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B}+\frac{1}{\left(\frac{W}{L}\right)_C}}+\frac{1}{\frac{1}{\left(\frac{W}{L}\right)_A}+\frac{1}{\left(\frac{W}{L}\right)_D+\left(\frac{W}{L}\right)_E}}$$

USING EULER PATH APPROACH





Stick-diagram, with arbitrary ordering of poly-Si

- The stick diagram layout ⇒ a "first attempt"
- An arbitrary ordering of the polysilicon gate column
  - The separation between polysilicon must be allow
    - One diffusion-to-diffusion separation
    - Two metal-to-diffusion contacts
  - Consuming area

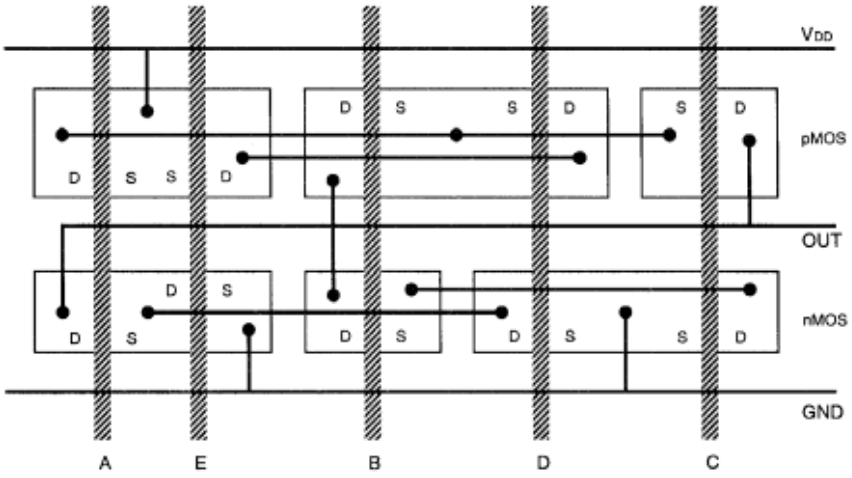
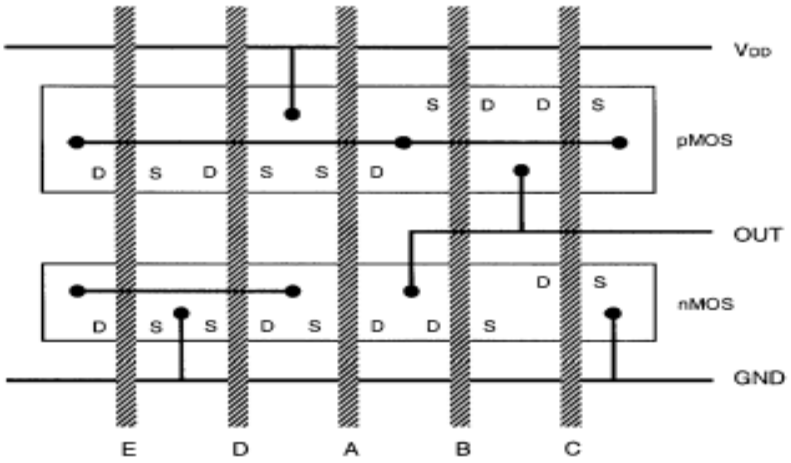


Figure Finding a common Euler path in both graphs for n-net and p-net provides a gate ordering that minimizes the number of diffusion breaks and, thus, minimizes the logic-gate layout area. In both cases, the Euler path starts at (x) and ends at (y).

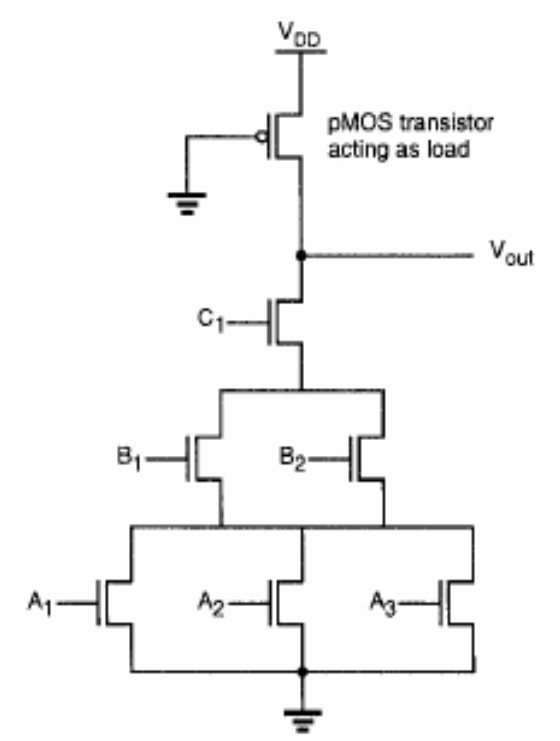


Optimized stick-diagram layout of the complex CMOS logic gate.

- Find a Euler-path in the pull-down graph and a Euler path in the pull-up graph with identical ordering of input labels
- The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once
  - E-D-A-B-C
- The polysilicon column separation has to allow
  - Only metal-to-diffusion contact
- More compact layout area, simple routing of signals, less parasitic capacitance

6. What is Pseudo nMOS logic? What are the advantages and disadvantages of Pseudo nMOS logic?

ANS:

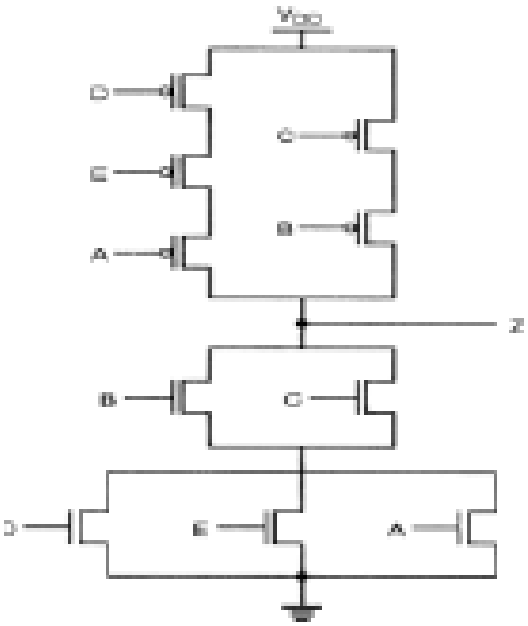


- CMOS gates ⇒ large area
- Pseudo-nMOS
  - To reduce the number of transistors
  - To use a single pMOS transistor as the load device
    - with its gate terminal connected to ground

- Disadvantage
  - Nonzero static power dissipation
    - As the V_{out} is lower than V_{DD} ⇒ the always-on pMOS load device conducts a steady state current
  - The value of V_{OL} and the noise margins
    - Determining by the ratio of pMOS transconductance load to driver transconductance

7. Find the $(W/L)_{n,Eqv}$ and $(W/L)_{p,Eqv}$ of the complex logic function $Z=\overline{(D+E+A)(B+C)}$ if $(W/L)_n$=10 for all nMOS and $(W/L)_p$ =15 for all pMOS.

Solution:



The Boolean function realized by this circuit is

$$Z = \overline{(D + E + A)(B + C)}$$

The equivalent (W/L) ratios of the nMOS network and the pMOS network are determined by using the series-parallel equivalency rules discussed earlier in this chapter, as follows.

$$\left(\frac{W}{L}\right)_{n,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D + \left(\frac{W}{L}\right)_E + \left(\frac{W}{L}\right)_A} + \frac{1}{\left(\frac{W}{L}\right)_B + \left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{30} + \frac{1}{20}} = 12$$

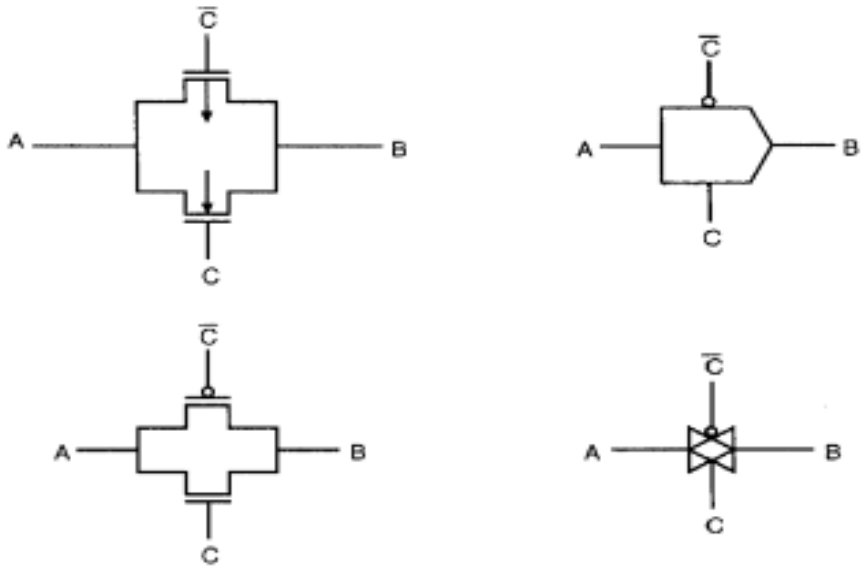
$$\left(\frac{W}{L}\right)_{p,eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_D} + \frac{1}{\left(\frac{W}{L}\right)_E} + \frac{1}{\left(\frac{W}{L}\right)_A}} + \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_B} + \frac{1}{\left(\frac{W}{L}\right)_C}}$$

$$= \frac{1}{\frac{1}{15} + \frac{1}{15} + \frac{1}{15}} + \frac{1}{\frac{1}{15} + \frac{1}{15}} = 12.5$$

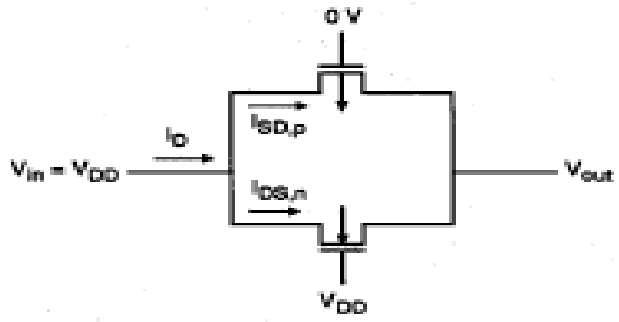
8. What are CMOS transmission gates ? Explain its operation with its symbols.

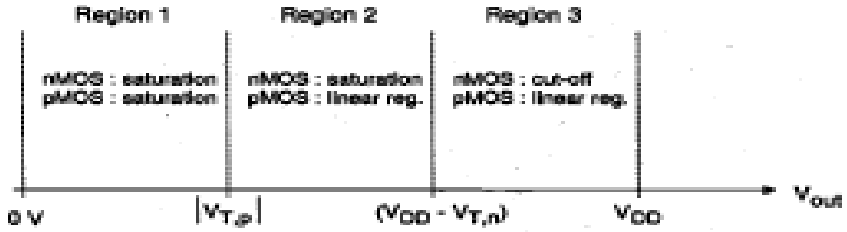
ANS:

- Consisting of one nMOS and one pMOS transistor, connected in parallel
- The gate voltage
  - Complementary signal to the two transistors
- Bidirectional switch between A and B, controlled by C
  - Signal C is logic-high
    - Both transistors turn on, low resistance current path
  - Signal C is logic-low
    - Both transistors turn off, open, high-impedance state
  - Substrate terminal
    - nMOS⇒ ground, pMOS ⇒ VDD
    - Must consider body effect



OPERATION:





$V_{in} = V_{DD}$, The control signal is logic - high, the output node may be connected to a capacitor

For *nMOS* transistor $\Rightarrow V_{DS,n} = V_{DD} - V_{out}$, $V_{GSn} = V_{DD} - V_{out}$

The *nMOS* will turn off for $V_{out} > V_{DD} - V_{T,n}$ and operate in the saturation for $V_{out} < V_{DD} - V_{T,n}$

For *pMOS* transistor $\Rightarrow V_{DS,p} = V_{out} - V_{DD}$, $V_{GS,p} = -V_{DD}$

The *pMOS* is in saturation for $V_{out} < |V_{T,p}|$, in linear region for $V_{out} > |V_{T,p}|$, *pMOS* remains turn on, regardless of the V_{out}

The total current : $I_D = I_{DS,n} + I_{SD,p}$

equivalent resistance : $R_{eq,n} = \dfrac{V_{DD} - V_{out}}{I_{DS,n}}$, $R_{eq,p} = \dfrac{V_{DD} - V_{out}}{I_{SD,p}}$, The total resistance = $R_{eq,n} \| R_{eq,p}$

Region 1

$V_{out} < |V_{T,p}| \Rightarrow$ both transistor in saturation, $R_{eq,n} = \dfrac{2(V_{DD} - V_{out})}{k_n (V_{DD} - V_{out} - V_{T,n})^2}$, $R_{eq,p} = \dfrac{2(V_{DD} - V_{out})}{k_p (V_{DD} - |V_{T,p}|)^2}$

note that $V_{SB,n} = V_{out}$, $V_{SB,p} = 0 \Rightarrow$ *nMOS* should take into account the sbustrate - bias effect

Region 2

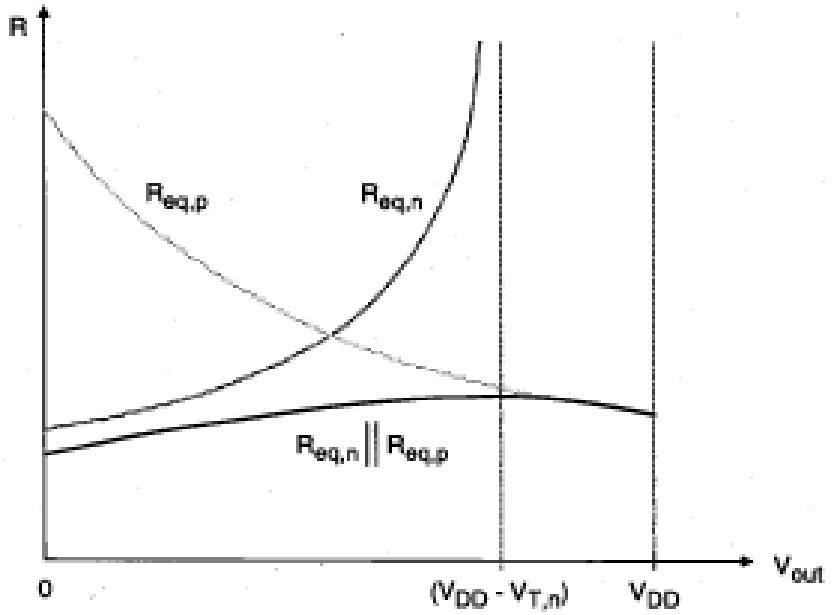
$|V_{T,p}| < V_{out} < (V_{DD} - V_{T,n}) \Rightarrow$ *pMOS* linear region, *nMOS* saturation region

$$R_{eq,n} = \frac{2(V_{DD} - V_{out})}{k_n (V_{DD} - V_{out} - V_{T,n})^2}, \quad R_{eq,p} = \frac{2(V_{DD} - V_{out})}{k_p \left[2(V_{DD} - |V_{T,p}|)(V_{DD} - V_{out}) - (V_{DD} - |V_{T,p}|)^2\right]} = \frac{2}{k_p \left[2(V_{DD} - |V_{T,p}|) - (V_{DD} - V_{out})\right]}$$

Region 3

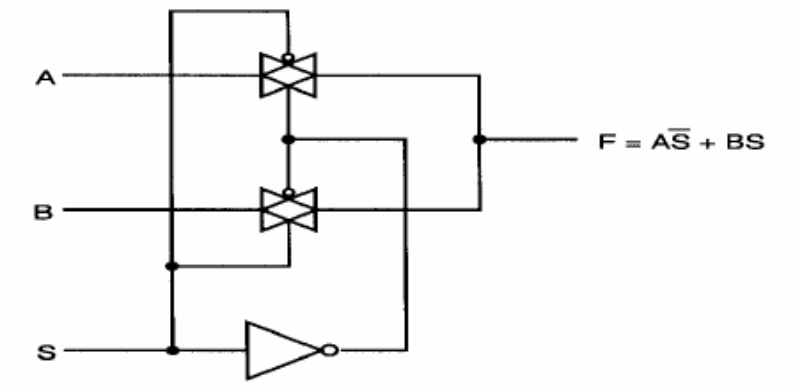
$V_{out} > (V_{DD} - V_{T,n}) \Rightarrow$ *pMOS* linear region, *nMOS* off

$$R_{eq,p} = \frac{2}{k_p \left[2(V_{DD} - |V_{T,p}|) - (V_{DD} - V_{out})\right]}$$



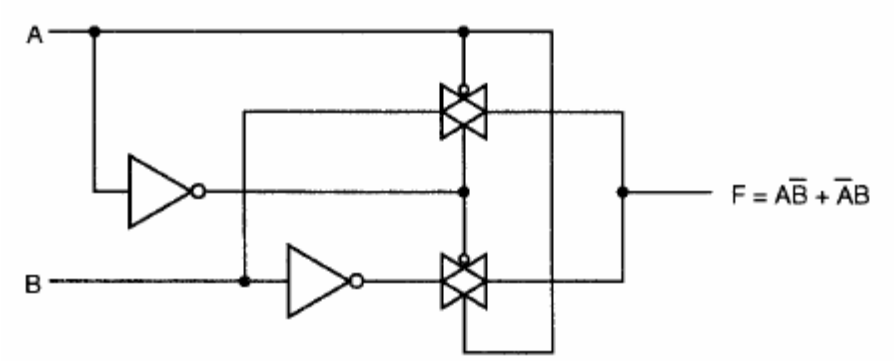
9. Design a 2-input MUX using transmission gate logic.

- The implement of CMOS transmission gates in logic circuit design
  - Compact circuit structures, requires a smaller number of transistors
  - The control signal and its complement must be available simultaneously for TG applications
- Two input multiplexer
  - If the control input S is logic high
    - The bottom TG conduct ⇒ output equal to the input B
  - If the control input S is logic low
    - The top TG conduct ⇒ output equal to the input A

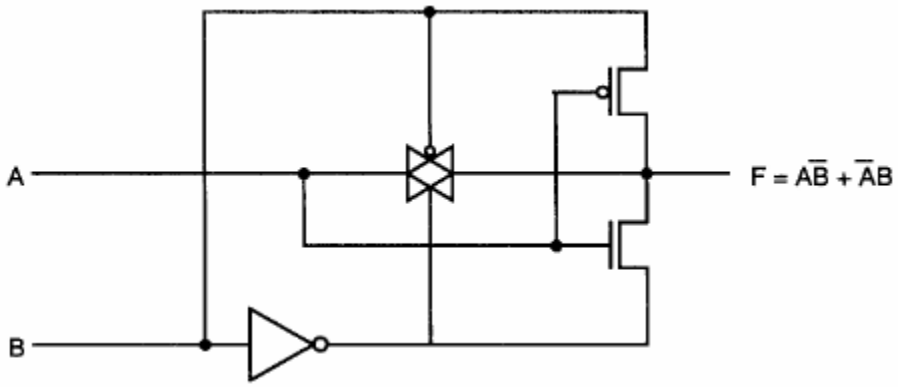


10. Design an XOR gate using transmission gate logic and using minimum number of transistor design the optimized XOR gate.

ANS:



Eight-transistor CMOS TG implementation of the XOR

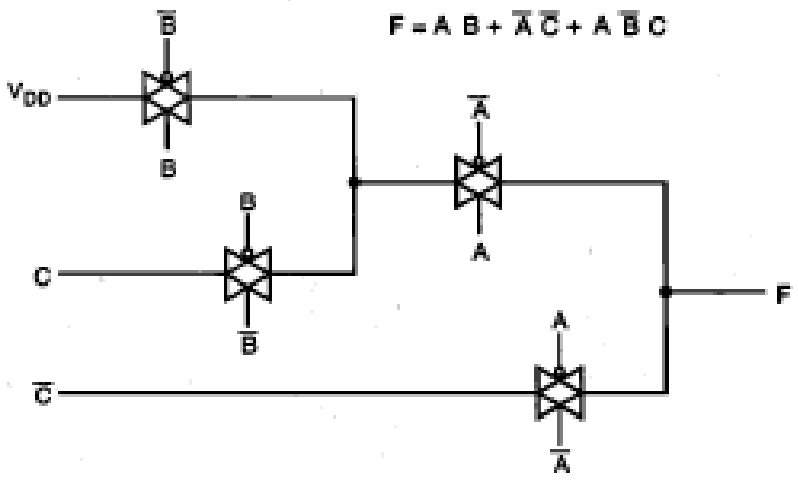


Six-transistor CMOS TG implementation of the XOR

11. Design the transmission gate implementation of a complex logic function:

$F = A\,B + \overline{A}\,\overline{C} + A\,\overline{B}\,C$

Solution:



12. What is Complementary pass transistor logic ? Design CPL NOR2 and CPL NAD2 gate . Write the advantages of CPL logic.

ANS:

- The main idea behind CPL is to use a purely nMOS pass-transistor network for the logic operations, instead of a CMOS TG network
  - All input are applied in complementary form
  - The circuit also produces complementary outputs, to be used by subsequent CPL stage
  - The CPL circuit consisting
    - Complementary input
    - An nMOS pass transistor logic network to generate complementary outputs
    - CMOS output inverter to restore the output signal

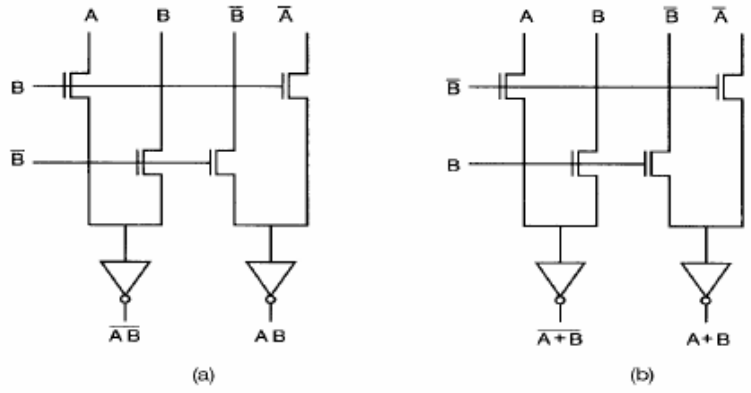


FIG: (a)CPL NAND2 gate (b) CPL NOR2 gate

ADVANTAGES:

- The elimination of pMOS transistors from the pass-gate network
  - Reducing the parasitic capacitances
  - Higher operation speed
  - Process complexity
    - The $V_{t,n}$ must be reduced to about 0V through threshold-adjustment implants
      - Reducing the overall noise immunity
      - Making the transistors more susceptible to subthreshold conduction in the off-mode
  - The CPL design style is highly modular
    - A wide range of functions can be realized by using the same basic pass-transistor structures

13. What are the advantages and disadvantages of pass transistor logic?

ANS:

Pass-Transistor Logic

- **Advantages**
- **Lower area due to smaller number of transistors and smaller input loads**
- **Ratio-less PTL allows minimum dimension transistors and hence makes area efficient circuit realization**
- **No short circuit current leading to lower power dissipation**

- **Disadvantages**
- **Increased delay due to long chain pf pass-transistors**
- **Multi-threshold voltage drop**
- **Dual-rail logic to provide all signals in complementary form**
- **There is possibility of sneak path**

Sequential MOS Logic Circuits

MULTIPLE CHOICE QUESTIONS

1. Clocked sequential circuits are
a) two phase overlapping clock
b) two phase non overlapping clock
c) four phase overlapping clock
d) four phase non overlapping clock

2. Which are easier to design?
a) clocked circuits
b) asynchronous sequential circuits
c) clocked circuits with buffer
d) asynchronous sequential circuits with buffers

3. As the temperature is increased, storage time _____
a) halved
b) doubled
c) does not change
d) tripled

4. Inverting dynamic register element consists of _____ transistors for nMOS and ____ for CMOS
a) two, three
b) three, two
c) three, four
d) four, three

5. Non inverting dynamic register storage cell consists of ____ transistors for nMOS and _____ for CMOS
a) six, eight
b) eight, six
c) five, six
d) six, five

6. Register cell consists of
a) inverter
b) pass transistor
c) both of the mentioned
d) none of the mentioned

7. In a four bit dynamic shift register basic nMOS transistor or inverters are connected in
a) series
b) cascade
c) parallel
d) series and parallel

8. In four bit dynamic shift register output is obtained
a) parallel output at inverters 1,3,5,7
b) parallel output at inverters 1,5,8
c) parallel output at all inverters
d) parallel output at inverter 2,4,6,8

9. For signals which are updated frequently _____ is used
a) static storage
b) dynamic storage
c) static and dynamic storage
d) buffer

10.

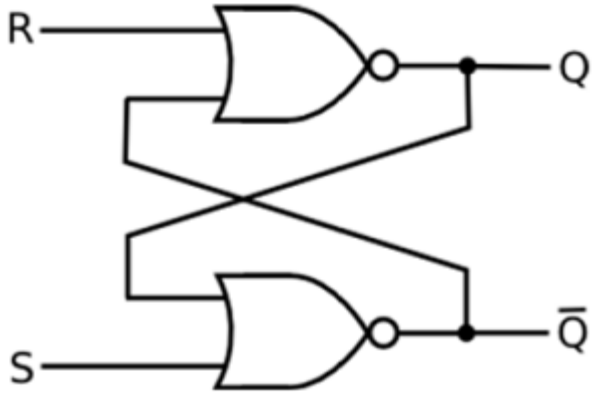
1(b),2(a),3(a), 4(c),5(a), 6(c), 7(b),8(d),9(b)

SUBJECTIVE QUESTIONS

Q-1. Describe SR Latch based on NOR gate and NAND gate using CMOS logic.

ANS:

SR Latch based on NOR Gate



If the set input (S) is equal to logic **"1"** and the reset input is equal to logic **"0."** then the output Q will be forced to logic **"1"**. While $\overline{Q}$ is forced to logic **"0"**. This means the SR latch will be set, irrespective of its previous state.

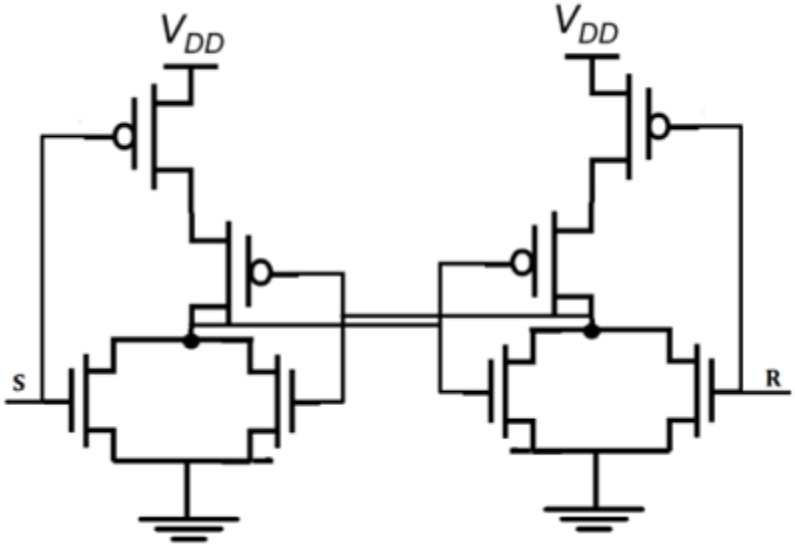
Similarly, if S is equal to "0" and R is equal to **"1"** then the output Q will be forced to **"0"** while $\overline{Q}$ is forced to **"1"**. This means the latch is reset, regardless of its previously held state. Finally, if both of the inputs S and R are equal to logic **"1"** then both output will be forced to logic **"0"** which conflicts with the complementarity of Q and $\overline{Q}$.

Therefore, this input combination is not allowed during normal operation. Truth table of NOR based SR Latch is given in table.

S	R	Q	$\overline{Q}$	Operation
0	0	Q	$\overline{Q}$	Hold
1	0	1	0	Set
0	1	0	1	Reset

1	1	0	0	Not allowed

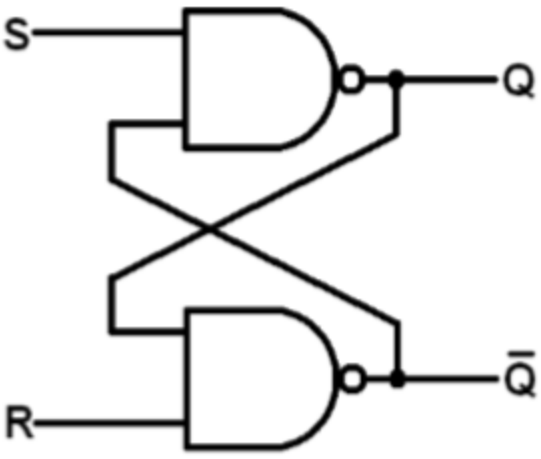
CMOS SR latch based on NOR gate is shown in the figure given below.



If the S is equal to V_{OH} and the R is equal to V_{OL}, both of the parallel-connected transistors M1 and M2 will be ON. The voltage on node $\overline{Q}$ will assume a logic-low level of $V_{OL} = 0$.

At the same time, both M3 and M4 are turned off, which results in a logic-high voltage V_{OH} at node Q. If the R is equal to V_{OH} and the S is equal to V_{OL}, M1 and M2 turned off and M3 and M4 turned on.

SR Latch based on NAND Gate



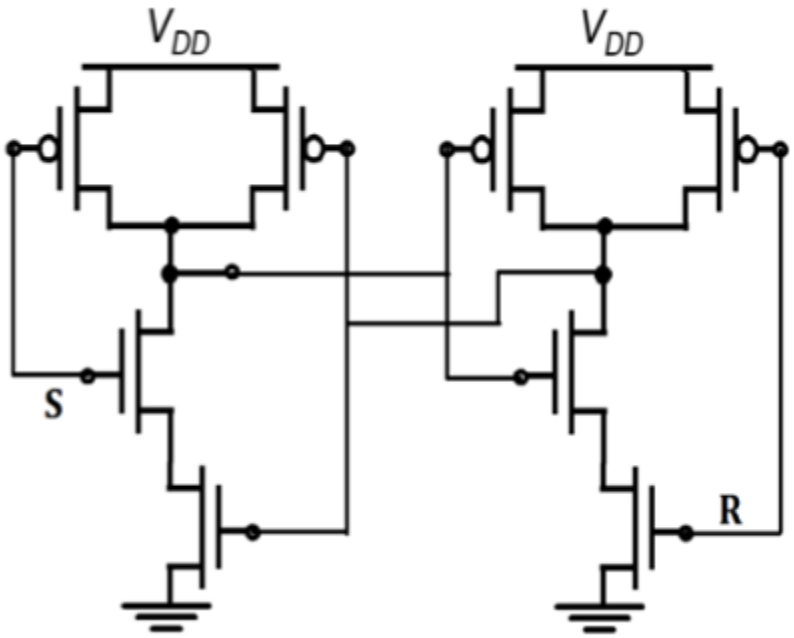
Block diagram and gate level schematic of NAND based SR latch is shown in the figure. The small circles at the S and R input terminals represents that the circuit responds to active low input signals. The truth table of NAND based SR latch is given in table

S	R	Q	Q′	
0	0	NC	NC	No change. Latch remained in present state.
1	0	1	0	Latch SET.
0	1	0	1	Latch RESET.
1	1	0	0	Invalid condition.

If S goes to 0 (while R = 1), Q goes high, pulling $\overline{Q}$ low and the latch enters Set state S = **0** then Q = **1** (if R = **1**)

If R goes to 0 (while S = 1), Q goes high, pulling $\overline{Q}$ low and the latch is Reset R = **0** then Q = **1** (if S = **1**)

Hold state requires both S and R to be high. If S = R = 0 then output is not allowed, as it would result in an indeterminate state. CMOS SR Latch based on NAND Gate is shown in figure.

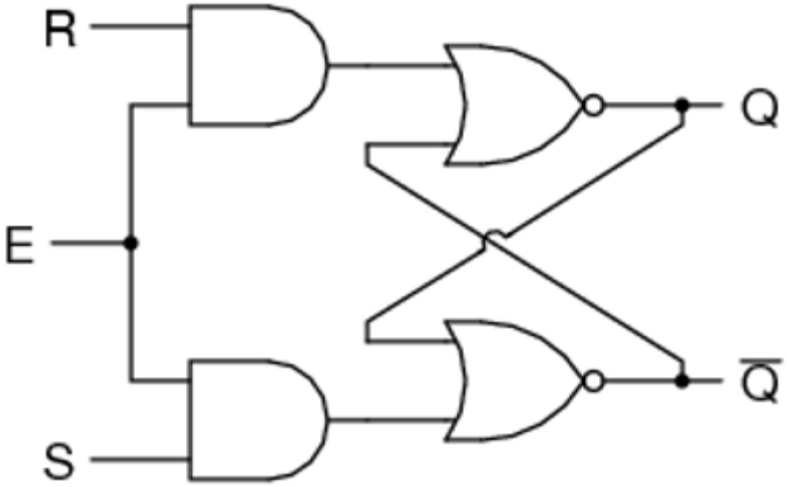


Depletion-load nMOS SR Latch based on NAND Gate is shown in figure. The operation is similar to that of CMOS NAND SR latch. The CMOS circuit implementation has low static power dissipation and high noise margin.

Q-2. Describe NOR based clocked SR latch .

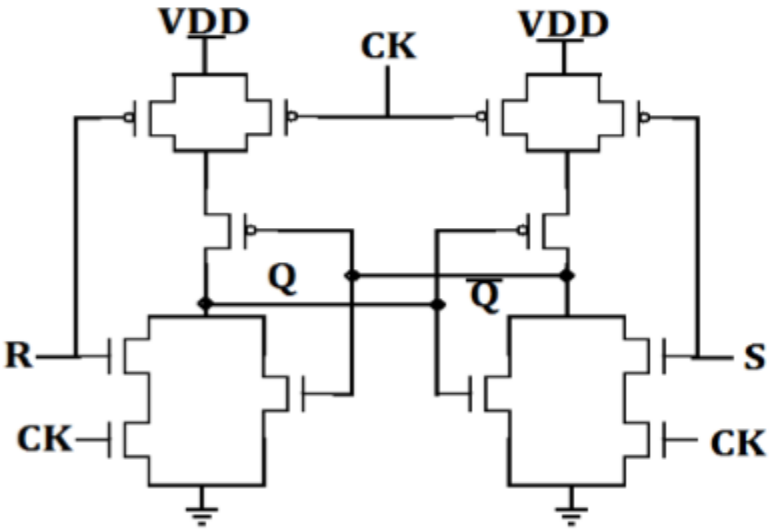
Clocked SR Latch

The figure shows a NOR-based SR latch with a clock added. The latch is responsive to inputs S and R only when CLK is high.



When CLK is low, the latch retains its current state. Observe that Q changes state −

- When S goes high during positive CLK.
- On leading CLK edge after changes in S & R during CLK low time.
- A positive glitch in S while CLK is high
- When R goes high during positive CLK.

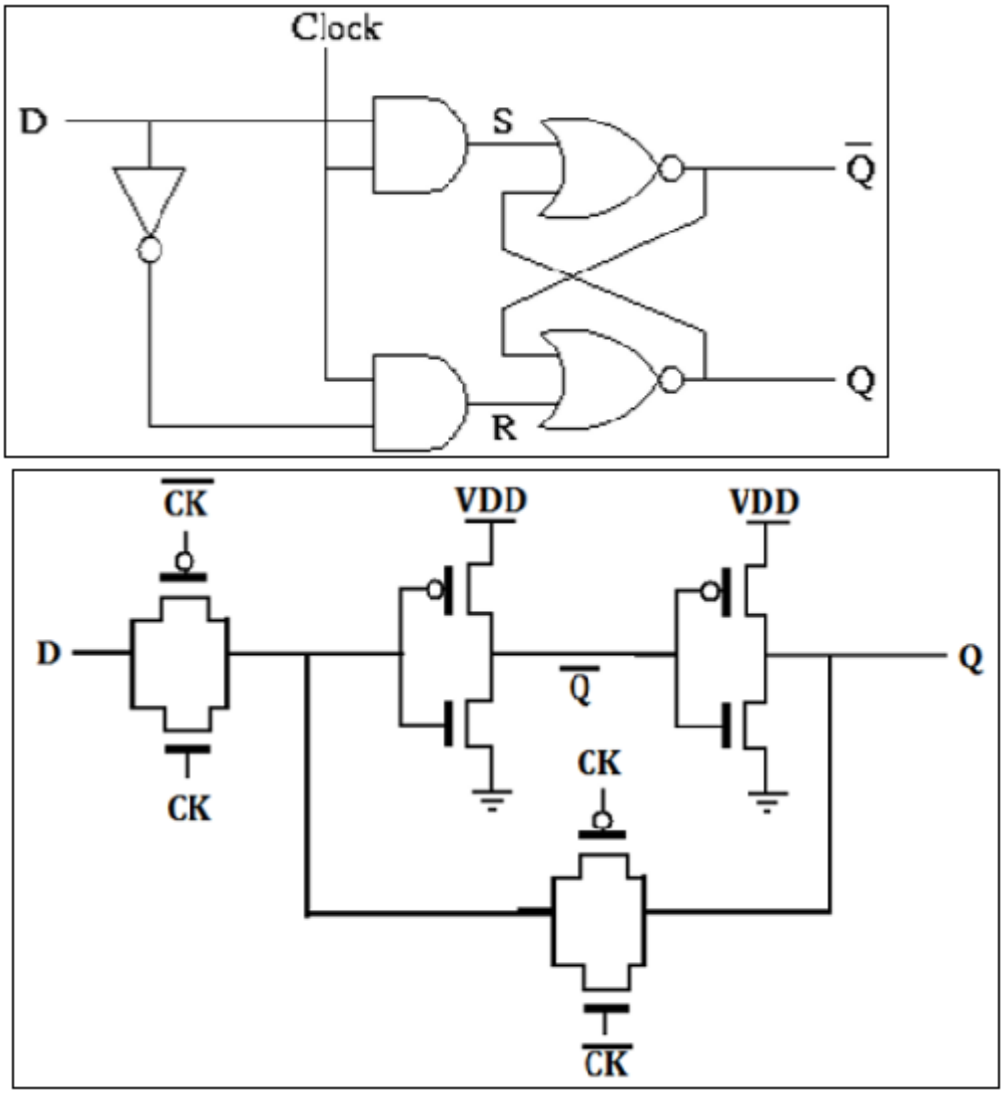


CMOS AOI implementation of clocked NOR based SR latch is shown in the figure. Note that only 12 transistors required.

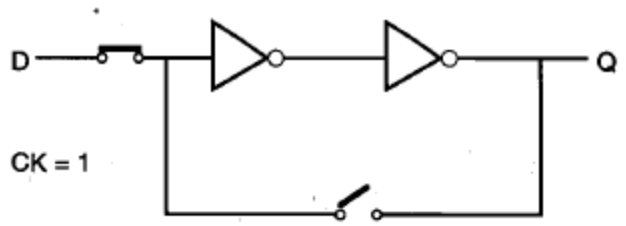
- When CLK is low, two series terminals in N tree N are open and two parallel transistors in tree P are ON, thus retaining state in the memory cell.
- When clock is high, the circuit becomes simply a NOR based CMOS latch which will respond to input S and R.

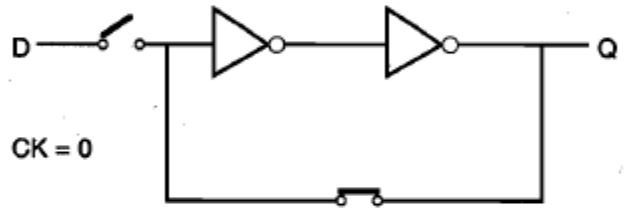
Q-3. Design CMOS D-latch implementation using pass transistor logic.

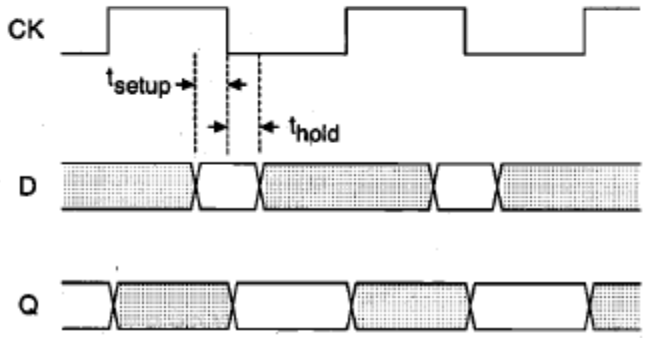
ANS:



The D latch is normally, implemented with transmission gate (TG) switches as shown in the figure. The input TG is activated with CLK while the latch feedback loop TG is activated with CLK. Input D is accepted when CLK is high. When CLK goes low, the input is open circuited and the latch is set with the prior data D.





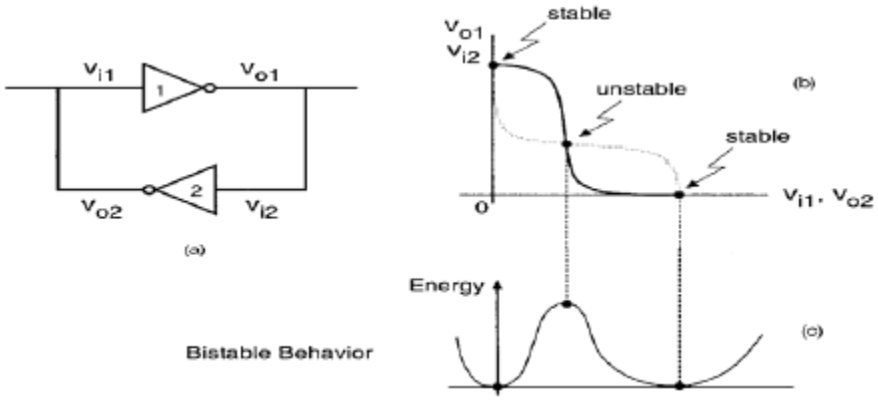


Q-4. Explain the behavior of bistable element.

ANS:

Behavior of bistable elements

- Two identical cross-coupled inverter circuits
  - $V_{o1}=V_{i2}$, $V_{o2}=V_{i1}$
  - The two voltage transfer characteristics, V_{o1}-V_{i1}, and V_{o2}-V_{i2}
    - Intersecting at three points
    - If the circuit is initially operating at one of these two stable point
      - Preserve this state unless it is forced externally to change its operating point
      - Gain is smaller than unity (at the two operating points)
        - » Need sufficiently large voltage perturbation
    - The third operating point
      - The voltage gains are larger than unity
      - A small perturbation at the input of any of the inverters will be amplified
      - Causing the operating to move to one of the stable operating point

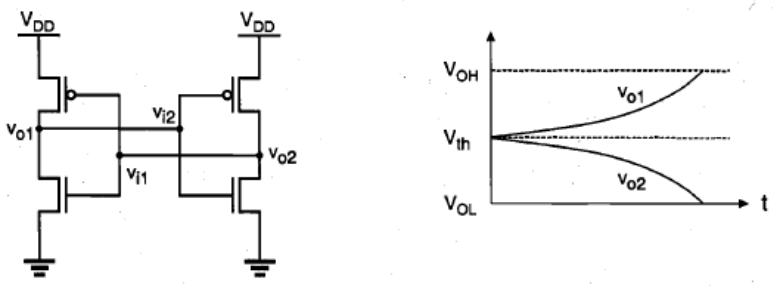


Q-5: Find out the small signal input output currents of a bistable element and find the output voltages.

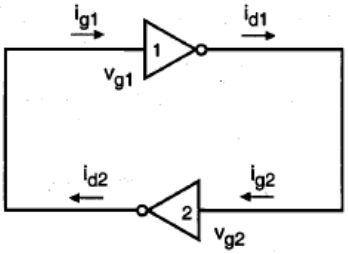
ANS:

- The bistable behavior of the cross-coupled inverter circuit can also be visualized qualitatively by examining the total potential energy level at each of the three possible operating points .
- It is seen that the potential energy is at its minimum at two of the three operating points, since the voltage gains of both inverters are equal to zero. By contrast, the energy attains a maximum at the operating point at which the voltage gains of both inverters are maximum.
- Thus, the circuit has two stable operating points corresponding to the two energy minima, and one unstable operating point corresponding to the potential energy maximum.

- Figure (1) shows the circuit diagram of a CMOS two-inverter bistable element. Here all four transistors are in saturation, resulting in maximum loop gain for the circuit. If the initial operating condition is set at this point, any small voltage perturbation will cause significant changes in the operating modes of the transistors. Thus, we expect the output voltages of the two inverters to diverge and eventually settle at V_{OH} and V_{OL}, respectively, as illustrated in Fig. 2. The direction in which each output voltage diverges is determined by the initial perturbation polarity.



- Using a small-signal analysis approach Consider the bistable circuit shown in Fig. 3, which is initially operating at $V_{o1}=V_{o2}=V_{th}$, i.e., at the unstable operating point. For our analysis, we will assume that the input (gate) capacitance C_g of each inverter is much larger than its output (drain) capacitance C_d, i.e., $C_g >> C_d$.



- The small-signal drain current supplied by each inverter (1 and 2) can be expressed, in terms of the small-signal gate voltage of that inverter, as follows.

$$i_{g1} = i_{d2} = g_m v_{g2}$$

$$i_{g2} = i_{d1} = g_m v_{g1}$$

- Note that the drain current of each inverter is also equal to the gate current of the other inverter.

$$v_{g1} = \frac{q_1}{C_g} \qquad v_{g2} = \frac{q_2}{C_g}$$

- Here, g_m represents the small-signal transconductance of the inverter. The gate voltages of both inverters can be expressed in terms of the gate charges, q_1 and q2.

$$g_m v_{g2} = C_g \frac{dv_{g1}}{dt}$$

$$g_m v_{g1} = C_g \frac{dv_{g2}}{dt}$$

- The small-signal gate current of each inverter can be written as a function of the time derivative of its small-signal gate voltage, as follows.

$$\frac{g_m}{C_g} q_2 = \frac{dq_1}{dt}$$

$$\frac{g_m}{C_g} q_1 = \frac{dq_2}{dt}$$

$$\frac{g_m}{C_g} q_1 = \frac{C_g}{g_m} \frac{d^2 q_1}{dt^2} \Rightarrow \qquad \frac{d^2 q_1}{dt^2} = \left(\frac{g_m}{C_g} \right)^2 q_1$$

$$\frac{d^2 q_1}{dt^2} = \frac{1}{\tau_0{}^2} q_1 \qquad \text{with } \tau_0 = \frac{C_g}{g_m}$$

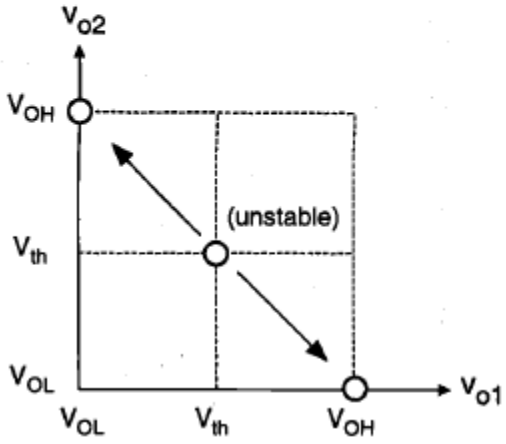
$$q_1(t) = \frac{q_1(0) - \tau_0 q_1'(0)}{2} e^{-\frac{t}{\tau_0}} + \frac{q_1(0) + \tau_0 q_1'(0)}{2} e^{+\frac{t}{\tau_0}}$$

$$v_{o2}(t) = \frac{1}{2}\left(v_{o2}(0) - \tau_0 v_{o2}'(0)\right) e^{-\frac{t}{\tau_0}} + \frac{1}{2}\left(v_{o2}(0) + \tau_0 v_{o2}'(0)\right) e^{+\frac{t}{\tau_0}}$$

$$v_{o1}(t) = \frac{1}{2}\left(v_{o1}(0) - \tau_0 v_{o1}'(0)\right) e^{-\frac{t}{\tau_0}} + \frac{1}{2}\left(v_{o1}(0) + \tau_0 v_{o1}'(0)\right) e^{+\frac{t}{\tau_0}}$$

v_{o1}: $V_{th} \rightarrow V_{OH}$ *or* V_{OL}

v_{o2}: $V_{th} \rightarrow V_{OL}$ *or* V_{OH}



Q6: Design a Clocked J K latch using NAND gates.

ANS:

The AOI-based circuit structure resulted in a relatively low transistor count

• There is no not-allowed input combination for the JK latch

• If J=1, K=1 during the active phase of the clock pulse

– The output of the circuit will oscillate (toggle) continuously until either the clock becomes inactive (goes to zero), or one of the input signal goes to zero

• To prevent this undesirable timing problem

– The clock pulse width must be made smaller than the input-to-output propagation delay of the JK latch circuit

– The clock signal must *go low* before the output level has an opportunity to switch again

– Assuming that the clock constrain above is satisfied

• The output of the JK latch will toggle (change its state) only once for each clock pulse, if both inputs are equal to logic "1"

• Toggle switch

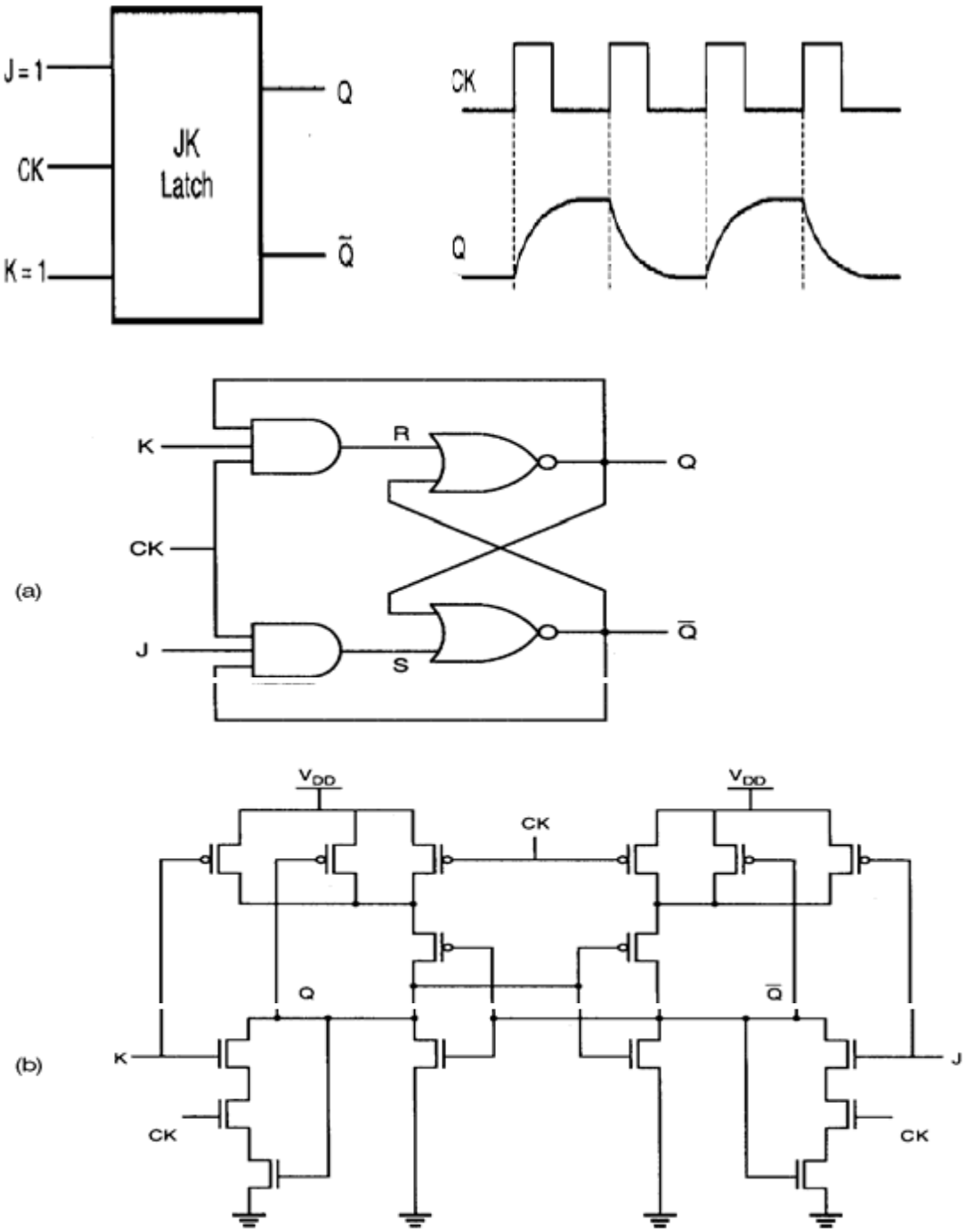


Figure 8.21 (a) Gate-level schematic of the clocked NOR-based JK latch circuit. (b) CMOS AOI realization of the JK latch.

Q-7. Design a NAND based master slave flip flop?
Ans:

• The master-slave flip-flop
– Most of the timing limitations encountered in the previously examined clocked latch circuits can be prevented by using two latch stages in a cascaded configuration
– The two cascaded stages are activated with opposite clock phases
• Operation
– Clock high
• The "master" is activated ⇒ the inputs J and K entered into the flip-flop ⇒ the first stage outputs are set according to the primarily inputs
– Clock goes to zero
• The "master" inactive, the "slave" active
• The output levels of the flip-flop circuit are determined during this second Phase

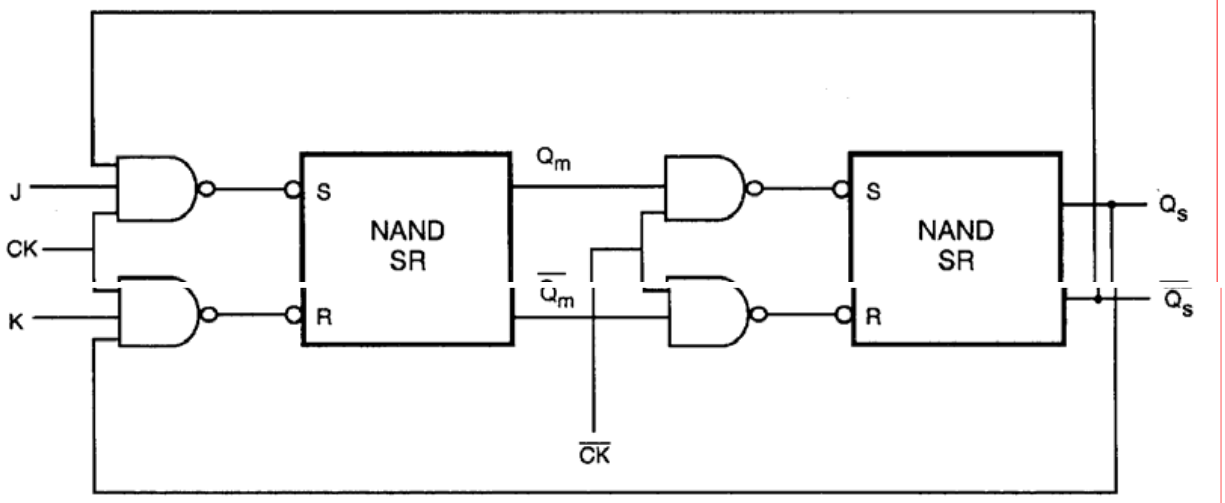


Figure 8.23 Master-slave flip-flop consisting of NAND-based JK latches.

The circuit is never transparent
– A change occurring in the primarily inputs is never reflected directly to the outputs
• Because the master and the slave stages are decoupled from each other, the circuits allows for toggling when J=K=1

• But it eliminates the possibility of the uncontrolled oscillations since only one stage is active at any given time.

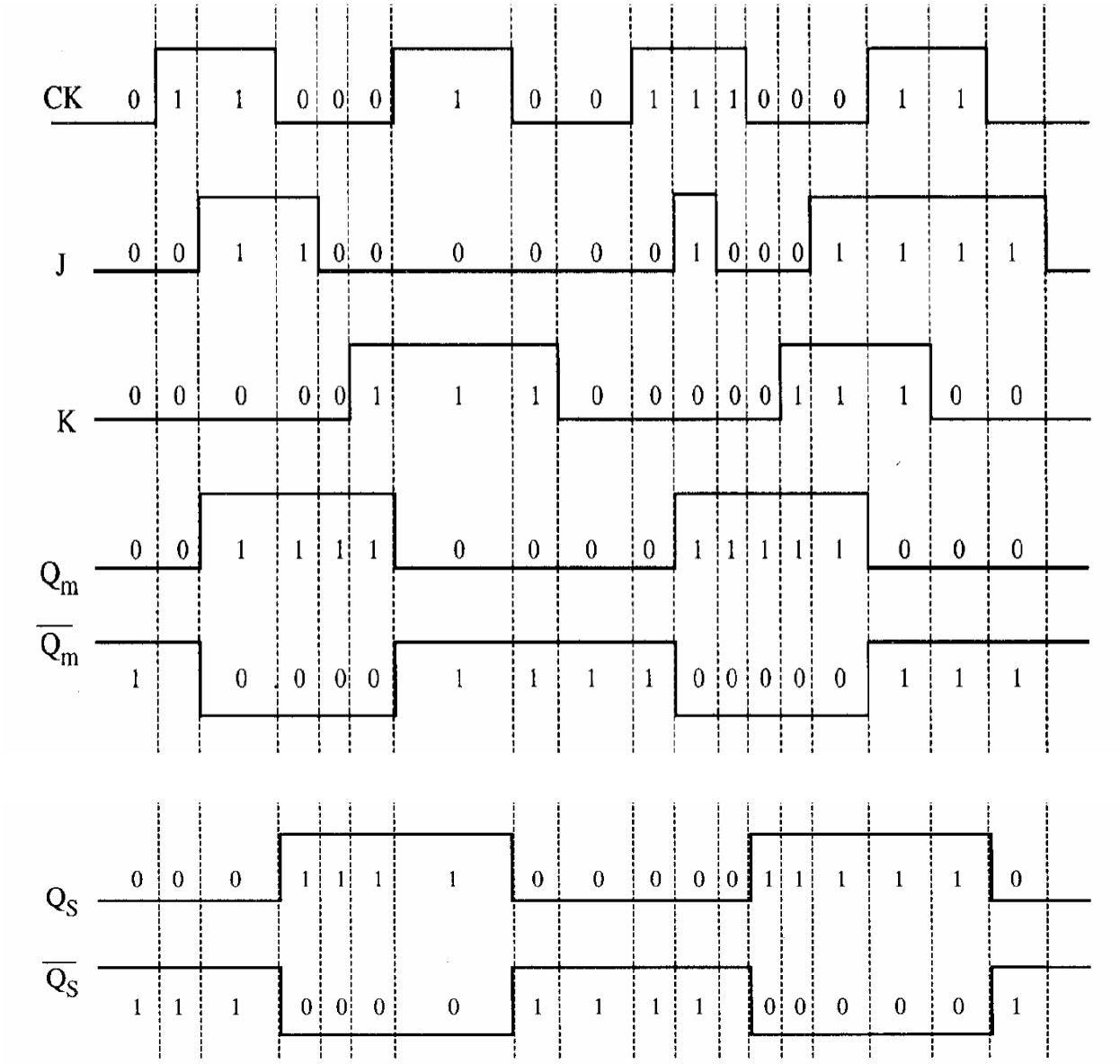


Figure 8.24 Sample input and output waveforms of the master-slave flip-flop circuit.

Dynamic Logic Circuits

MULTIPLE CHOICE QUESTIONS

1. Output of DOMINO CMOS gate is low at beginning of
   a) precharge phase
   b) evaluation phase
   c) dynamic phase
   d) static phase

2. Design of address decoders in memory chips can be done in
   a) TTL logic
   b) PTL logic
   c) DOMINO CMOS Logic
   d) CMOS logic

3. At rising edge of clock, output will make
   a) 0-1 transition
   b) 1-0 transition
   c) z-0 transition
   d) z-1 transition

4. As output of DOMINO CMOS gate is low, premature capacitance will
   a) charge
   b) discharge
   c) doesn't change
   d) remains constant

5. A form of dynamic logic that result in cascaded gates is termed as
   a) TTL logic
   b) PTL logic
   c) DOMINO CMOS Logic
   d) CMOS logic

6. Which transistor passes strong “1” and weaker “0”?
   a) nMOS
   b) pMOS
   c) cMOS

d) None

7. The two phases of Dynamic logic are
   a) precharge and evaluate
   b) 0 phase and 1 phase
   c) charge up and charge down phase
   d) None

8. How the threshold voltage can be optimized in dynamic logic
  a) Voltage divider
 b) ring oscillator
 c) voltage bootstrapping
 d) None

9. In dynamic logic when clock signal is high PMOS turned off and single NMOS at PDN will
 a) turned off
b) turned on
c) does not change
d) goes to breakdown region

10. Low noise margin for dynamic logic circuit =
a) 5v
b) 3V
c)threshold voltage
d)input voltage

11. Output of domino CMOS logic is low at beginning of
a) precharge phase
b)evaluation phase
c)dynamic phase
d)static phase

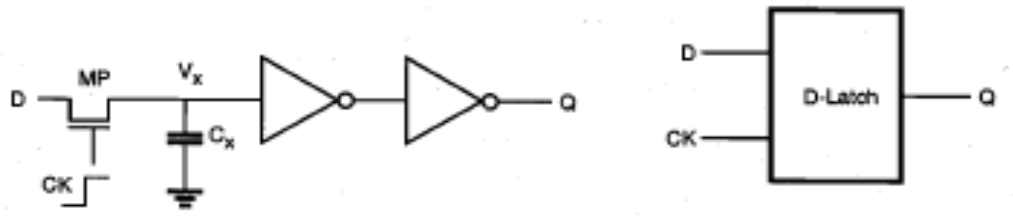
12. High noise margin for dynamic logic circuits=
a) V_{DD}- V_{th}
b) 3V
c) threshold voltage

d) input voltage

ANSWER KEY: 1(b),2(c), 3(c),4(c),5(c), 6(b),7(a), 8(c),9(b), 10(c), 11(b), 12(a)

SUBJECTIVE QUESTIONS

1. **Consider the dynamic D-latch circuit shown below. The circuit consists of two cascaded inverters and one nMOS pass transistor driving the input of the primary inverter stage. Explain how the parasitic input capacitance plays an important role in the dynamic behavior of the circuit.**



ANS:

We will see that the parasitic input capacitance C. of the primary inverter stage plays an important role in the dynamic operation of this circuit. The input pass transistor is being driven by the external periodic clock signal, as follows:

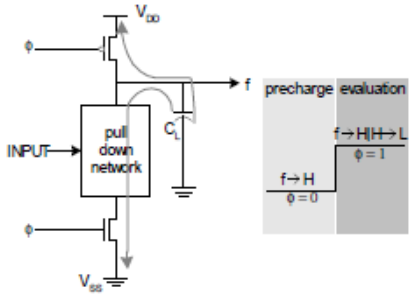
* When the clock is high (CK = 1), the pass transistor turns on. The capacitor *C,* is either charged up, or charged down through the pass transistor MP, depending on the input (D) voltage level. The output (Q) assumes the same logic level as the input.

* When the clock is low (CK = 0), the pass transistor MP turns off, and the capacitor C is isolated from the input D. Since there is no current path from the intermediate node X to either *VDD* or ground, the amount of charge stored in C. during the previous cycle determines the output voltage level Q.

2. What are the advantages and disadvantages of Dynamic Logic?

ANS:

Dynamic CMOS Logic



- Advantages
  - Combines the advantages of low power of static CMOS and low chip area of pseudo-nMOS
  - Reduced number of transistors compared to static CMOS (n+2 versus 2n)
  - Faster than static CMOS logic
  - No short circuit power dissipation
  - No spurious transition and glitching power dissipation

- Disadvantages
  - Higher switching activity
  - Not as robust as static CMOS logic
  - Clock skew problem in cascaded realization
  - Suffers from charge sharing problem
  - Mature synthesis tool not available

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3. What are the basic principles of pass transistor logic?

Ans:

- The fundamental building block of nMOS dynamic logic circuits, consisting of an nMOS pass transistor driving the gate of another nMOS transistor, is shown in Fig. 1.

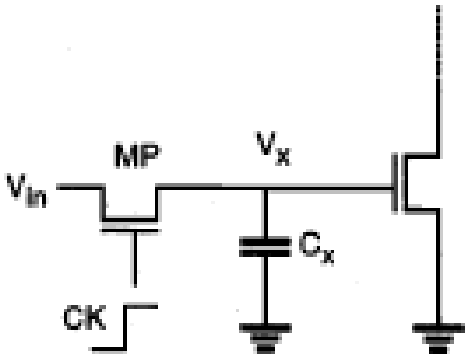


Fig.1: Basic building block of nMOS dynamic logic

- The pass transistor MP is driven by the periodic clock signal and acts as an access switch to either charge up or charge down the parasitic capacitance C_x, depending on the input signal V_{in}. Thus, the two possible operations when the clock signal is active (CK = 1) are the logic " 1 " transfer (charging up the capacitance C_X to a logic-high level) and the logic "0" transfer (charging down the capacitance C_X to a logic-low level). In either case, the output of the depletion-load nMOS inverter obviously assumes a logic-low or a logic-high level, depending on the voltage V_X.

Logic "1" Transfer

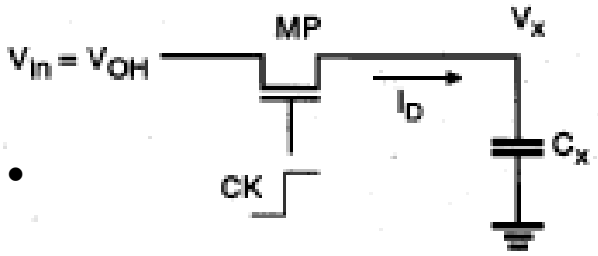


Fig.2: Equivalent circuit for the logic " 1 " transfer event.

- Assume that the soft node voltage is equal to 0 initially, i.e., $Vx(t = 0) = 0$ V. A logic " 1" level is applied to the input terminal, which corresponds to $V_{in} = V_{OH} = V_{DD}$. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at t = 0. It can be seen that the pass transistor MP starts to conduct as soon as the clock signal becomes active and that MP will operate in saturation throughout this cycle since $V_{DS} = V_{GS}$.

- Consequently, $V_{Ds} > V_{GS} - V_{TN}$. The circuit to be analyzed for the logic 1 " transfer event can be simplified into an equivalent circuit as shown in Fig. 2.
- A logic " 1" level is applied to the input terminal, which corresponds to $V_{in} = V_{OH} = V_{DD}$. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at t = 0.
- It can be seen that the pass transistor MP starts to conduct as soon as the clock signal becomes active and that MP will operate in saturation throughout this cycle since $V_{DS} = V_{GS}$.
- Consequently, $V_{Ds} > V_{GS} - V_{TN}$. The circuit to be analyzed for the logic 1 " transfer event can be simplified into an equivalent circuit as shown in Fig.2.

$$C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(V_{DD} - V_x - V_{T,n}\right)^2$$

$$\int_0^t dt = \frac{2C_x}{k_n}\int_0^{V_x} \frac{dV_x}{\left(V_{DD} - V_x - V_{T,n}\right)^2}$$

$$= \frac{2C_x}{k_n}\left(\frac{1}{\left(V_{DD} - V_x - V_{T,n}\right)}\right)\Bigg|_0^{V_x}$$

$$t = \frac{2C_x}{k_n}\left[\left(\frac{1}{V_{DD} - V_x - V_{T,n}}\right) - \left(\frac{1}{V_{DD} - V_{T,n}}\right)\right]$$

$$V_x(t) = \left(V_{DD} - V_{T,n}\right)\frac{\left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t}{1 + \left(\frac{k_n\left(V_{DD} - V_{T,n}\right)}{2C_x}\right)t}$$

The variation of the node voltage V is plotted as a function of time in Fig. 3. The voltage rises from its initial value of 0 V and approaches a limit value for large t, but it cannot exceed its limit value of V = ($V_{DD} - V_{TN}$). The pass transistor will turn off at $V_x = V_{max}$, since at this point, its gate-to-source voltage will be equal to its threshold voltage. Therefore, the voltage at node X can never attain the full power supply I voltage level of V_{DD} during the logic "1" transfer. The actual value of the maximum 1 possible voltage V at node X can be found by taking into account the substrate bias effect for MP.

$$V_{max} = V_x|_{t\to\infty} = V_{DD} - V_{T,n}$$
$$= V_{DD} - V_{T0,n} - \gamma\left(\sqrt{|2\phi_F| + V_{max}} - \sqrt{|2\phi_F|}\right)$$

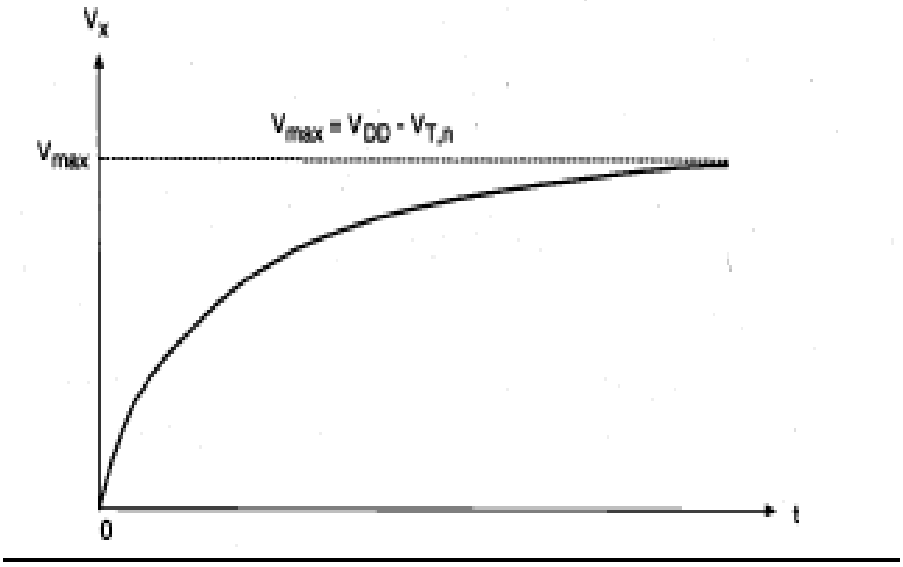


Figure 3. Variation of V as a function of time during logic "I" transfer.

Logic "0" Transfer

- Assume that the soft-node voltage V is equal to a logic " 1 " level initially, i.e., $V(t = 0) = V_{max} = (V_{DD} - V_{Tn})$.
- A logic "0" level is applied to the input terminal, which corresponds to $V_{in} = 0$ V. Now, the clock signal at the gate of the pass transistor goes from 0 to V_{DD} at t = 0.
- The pass transistor MP starts to conduct as soon as the clock signal becomes active, and the direction of drain current flow through MP will be opposite to that during the charge-up (logic " 1 " transfer) event. This means that the intermediate node X will now correspond to the drain terminal of MP and that the input node will correspond to its source terminal.

- With $V_{GS} = V_{DD}$ and $V_{DS} = V_{max}$, it can be seen that the pass transistor operates in the linear region throughout this cycle, since $V_{DS} < V_{GS} - V_{Tn}$.
- The circuit to be analyzed for the logic "0" transfer event can be simplified into an equivalent circuit as shown in Fig. 4. As in the logic " 1 " transfer case, the depletion load nMOS inverter does not affect this event.

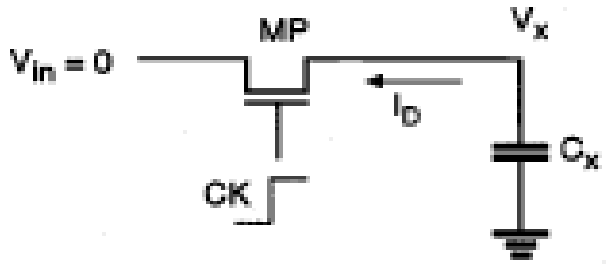


Fig.4: Equivalent circuit for the logic "0" transfer event.

- The pass transistor MP operating in the linear region discharges the parasitic capacitor C_x, as follows:

$$-C_x \frac{dV_x}{dt} = \frac{k_n}{2}\left(2\left(V_{DD} - V_{T,n}\right)V_x - V_x^2\right)$$

$$dt = -\frac{2C_x}{k_n} \cdot \frac{dV_x}{2\left(V_{DD} - V_{T,n}\right)V_x - V_x^2}$$

Note that the source voltage of the nMOS pass transistor is equal to 0 V during this event; hence, there is no substrate bias effect for MP ($V_{Tn} = V_{To,n}$). But the initial condition

- $V(t = 0) = (V_{DD} - V_{Tn})$ contains the threshold voltage with substrate bias effect, because the voltage V is set during the preceding logic "1" transfer event. To simplify the expressions, we will use V_{Tn} in the following.

$$\int_0^t dt = -\frac{2C_x}{k_n}\int_{V_{DD}-V_{T,n}}^{V_x}\left(\frac{\frac{1}{2\left(V_{DD}-V_{T,n}\right)}}{2\left(V_{DD}-V_{T,n}\right)-V_x} + \frac{\frac{1}{2\left(V_{DD}-V_{T,n}\right)}}{V_x}\right)dV_x$$

$$t = \frac{C_x}{k_n\left(V_{DD}-V_{T,n}\right)}\left[\ln\left(\frac{2\left(V_{DD}-V_{T,n}\right)-V_x}{V_x}\right)\right]\Bigg|_{V_{DD}-V_{T,n}}^{V_x}$$

$$t = \frac{C_x}{k_n (V_{DD} - V_{T,n})} \ln\left(\frac{2(V_{DD} - V_{T,n}) - V_x}{V_x}\right)$$

The variation of the node voltage V_x is plotted as a function of time in Fig. 5. It is seen that the voltage drops from its logic-high level of V_{max} to V. Hence, unlike the charge-up case, the applied input voltage level (logic 0) can be transferred to the soft node without any modification during this event.

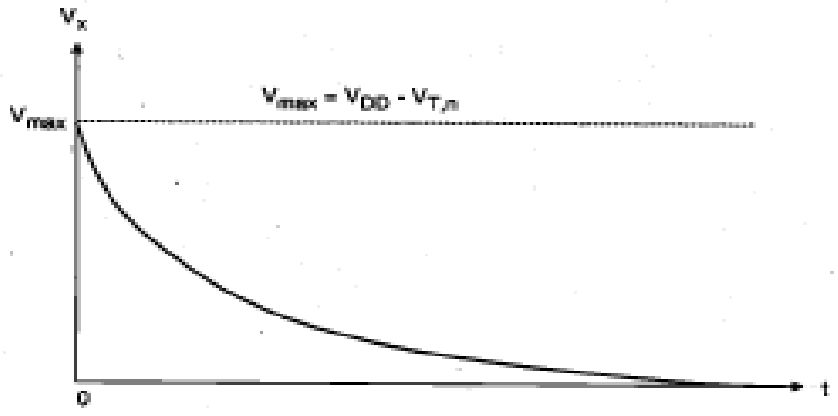


Fig.5: Variation of V_x as a function of time during logic "0" transfer.

Q-4. Explain charge leakage concept of dynamic circuitsat the soft node point.

ANS:

The preservation of a correct logic level at the soft node during the inactive clock phase depends on preserving a sufficient amount of charge in. C_X , despite the leakage currents. We will assume that a logic-high voltage level has been transferred to the soft node during the active clock phase and that now both the input voltage V_{in} and the clock are equal to 0 V. The charge stored in $\boldsymbol{C_x}$ will gradually leak away, primarily due to the leakage currents associated with the pass transistor. The gate current of the inverter driver transistor is negligible for all practical purposes.

Figure 1 shows a simplified cross-section of the nMOS pass transistor, together with the lumped node capacitance C_x. We see that the leakage current responsible for draining the soft-node capacitance over time has two main components,

namely, the subthreshold channel current and the reverse conduction current of the drain-substrate junction.

$$I_{leakage} = I_{subthreshold(MP)} + I_{reverse(MP)}$$

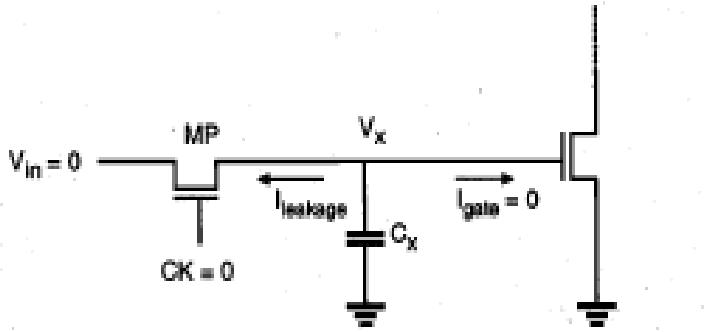


Fig1: Charge leakage from the soft node.

Note that a certain portion of the total soft-node capacitance C_x is due to the reverse biased drain-substrate junction, which is also a function of the soft-node voltage V. Other components of C_x which are primarily due to oxide-related parasitics, can be considered constants. In our analysis, these constant capacitance components will be represented by C_{in} (Fig. 3). Thus, we have to express the total charge stored in the soft node as the sum of two main components, as follows.

$$Q = Q_j(V_x) + Q_{in} \quad \text{where} \quad Q_{in} = C_{in} \cdot V_x$$

$$C_{in} = C_{gb} + C_{poly} + C_{metal}$$

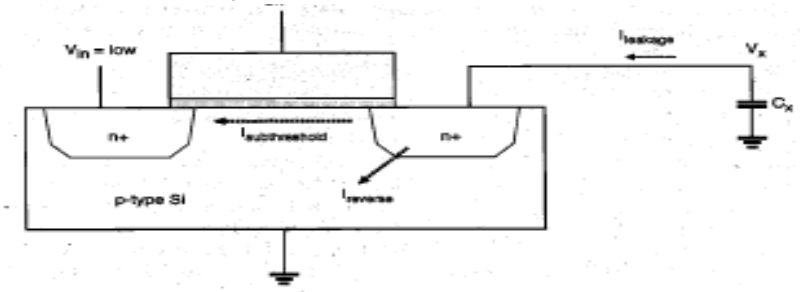


Fig.2: Simplified cross-section of the nMOS pass transistor, showing the leakage current components responsible for draining the soft-node capacitance C_x.

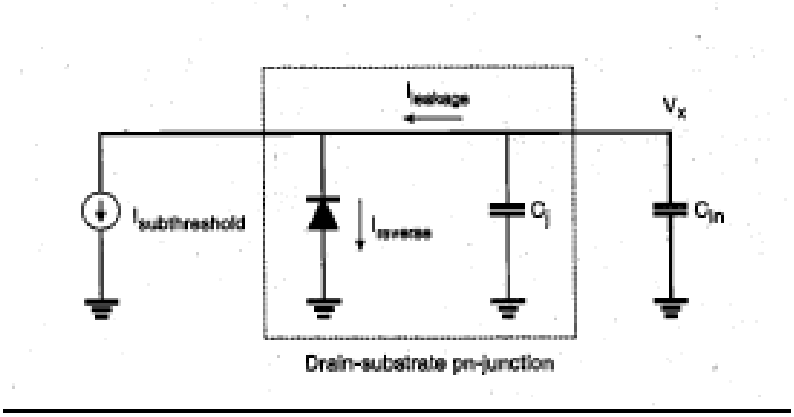
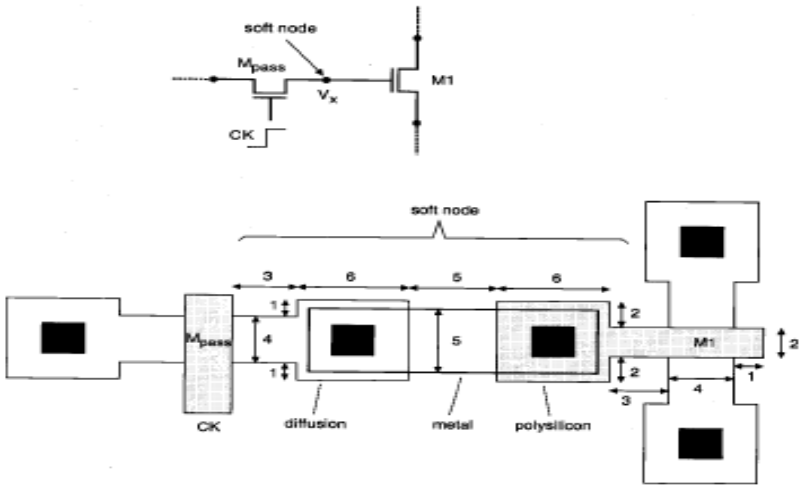


Fig3: Equivalent circuit used for analyzing the charge leakage process.

The total leakage current can be expressed as the time derivative of the total soft-node charge Q.

$$I_{leakage} = \frac{dQ}{dt}$$
$$= \frac{dQ_j(V_x)}{dt} + \frac{dQ_{in}}{dt}$$
$$= \frac{dQ_j(V_x)}{dV_x}\frac{dV_x}{dt} + C_{in}\frac{dV_x}{dt}$$

<u>Q-5:</u> Consider the soft-node structure shown below, which consists of the drain (or source, depending on current direction) terminal of the pass transistor, connected to the polysilicon gate of an nMOS driver transistor via a metal interconnect.



We will assume that the power supply voltage used in this circuit is V_{DD} = V, and that the soft node has initially been charged up to its maximum voltage, V.. In order to estimate the worst-case holding time, the total soft-node capacitance must be calculated first. The simplified mask layout of the structure is shown in the following. All dimensions are given in micrometers. The critical material parameters to be used in this example are listed below. Find the leakage current and hold time.

SOLUTION:

$$V_{T0} = 0.8 \text{ V}$$
$$\gamma = 0.4 \text{ V}^{1/2}$$
$$|2\phi_F| = 0.6 \text{ V}$$

$$C_{ox} = 0.065 \text{ fF}/\mu\text{m}^2$$
$$C_{metal} = 0.036 \text{ fF}/\mu\text{m}^2$$
$$C_{poly} = 0.055 \text{ fF}/\mu\text{m}^2$$
$$C_{j0} = 0.095 \text{ fF}/\mu\text{m}^2$$
$$C_{j0sw} = 0.2 \text{ fF}/\mu\text{m}$$

$$C_{gb} = C_{ox} \cdot W \cdot L_{mask}$$
$$= 0.065 \text{ fF}/\mu\text{m}^2 \cdot (4 \ \mu\text{m} \times 2 \ \mu\text{m})$$
$$= 0.52 \text{ fF}$$

$$C_{metal} = 0.036 \text{ fF}/\mu\text{m}^2 \cdot (5 \ \mu\text{m} \times 5 \ \mu\text{m})$$
$$= 0.90 \text{ fF}$$

$$C_{poly} = 0.055 \text{ fF}/\mu\text{m}^2 \cdot (36 \ \mu\text{m}^2 + 8 \ \mu\text{m}^2)$$
$$= 2.42 \text{ fF}$$

$$C_{db,max} = C_{bottom} + C_{sidewall}$$
$$= A_{bottom} \cdot C_{j0} + P_{sidewall} \cdot C_{j0sw}$$
$$= (36 \ \mu\text{m}^2 + 12 \ \mu\text{m}^2) \cdot 0.095 \text{ fF}/\mu\text{m}^2 + 30 \ \mu\text{m} \cdot 0.2 \text{ fF}/\mu\text{m}$$
$$= 4.56 \text{ fF} + 6.0 \text{ fF}$$
$$= 10.56 \text{ fF}$$

$$V_{max} = 5.0 - 0.8 - 0.4\left(\sqrt{0.6 + V_{max}} - \sqrt{0.6}\right)$$

$$\Rightarrow V_{max} = 3.68 \text{ V}$$

$$C_{db,min} = \frac{C_{bottom}}{\sqrt{1+\frac{V_{x,max}}{\phi_0}}} + \frac{C_{sidewall}}{\sqrt{1+\frac{V_{x,max}}{\phi_{0sw}}}}$$
$$= \frac{4.56\ \text{fF}}{\sqrt{1+\frac{3.68}{0.88}}} + \frac{6.0\ \text{fF}}{\sqrt{1+\frac{3.68}{0.95}}} = 4.71\ \text{fF}$$

$$C_{x,min} = C_{gb} + C_{metal} + C_{poly} + C_{db,min}$$
$$= 0.52\ \text{fF} + 0.90\ \text{fF} + 2.42\ \text{fF} + 4.71\ \text{fF}$$
$$= 8.55\ \text{fF}$$

$$\Delta Q_{critical} = C_{x,min} \cdot \left(V_{x,max} - \frac{V_{DD}}{2} \right)$$
$$= 8.55\ \text{fF} \cdot (3.68\ \text{V} - 2.5\ \text{V})$$
$$= 10.09\ \text{fC}$$

$$I_{leakage} = I_{subthreshold} + I_{reverse} = 0.85\ \text{pA}$$

$$t_{hold,min} = \frac{\Delta Q_{critical}}{I_{leakage,max}}$$
$$= \frac{10.09\ \text{fC}}{0.85\ \text{pA}} = \underline{11.87\ \text{ms}}$$

Q-6: What is voltage bootstrapping? Explain briefly the use of voltage bootstrapping in dynamic circuits.

ANS:

Dynamic voltage bootstrapping techniques offer a simple yet effective way to overcome threshold voltage drops which occur in most situations. Consider the circuit shown in Fig. 1, where the voltage Vx is equal to or smaller than the power supply voltage, $Vx < V_{DD}$. Consequently, the enhancement-type nMOS transistor M2 will operate in saturation. When the input voltage V_{in} is low, the maximum value that the output voltage can attain is limited by

$$V_{out}(max) = V_x - V_{T2}(V_{out})$$

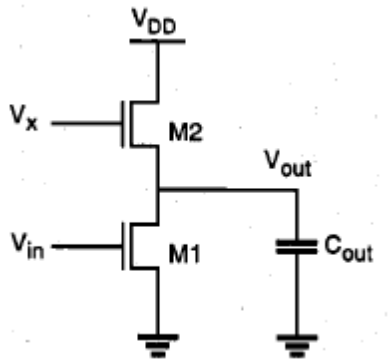


Figure 1. Enhancement-type circuit in which the output node is weakly driven.

To overcome the threshold voltage drop and to obtain a full logic-high level *(V_{DD})* at the output node, the voltage V must be increased.

Now consider the circuit shown in Fig. 9.12, where a third transistor M3 has been added to the circuit. The two capacitors C_s and C_{boot}, seen in the circuit diagram represent the capacitances which dynamically couple the voltage V. to the ground and to the output, respectively. We will see that this circuit can produce a high V_x during switching, so that the threshold voltage drop can be overcome at the output node.

$$V_x \geq V_{DD} + V_{T2}(V_{out})$$

Initially assume that the input voltage V_{in} is logic-high, so that MI and M2 have a nonzero drain current and that the output voltage is low. At this point, MI is in the linear' region and M2 is in saturation. Since $I_{D3} = 0$, the initial condition for the voltage Vx can be found as

$$V_x = V_{DD} - V_{T3}(V_x)$$

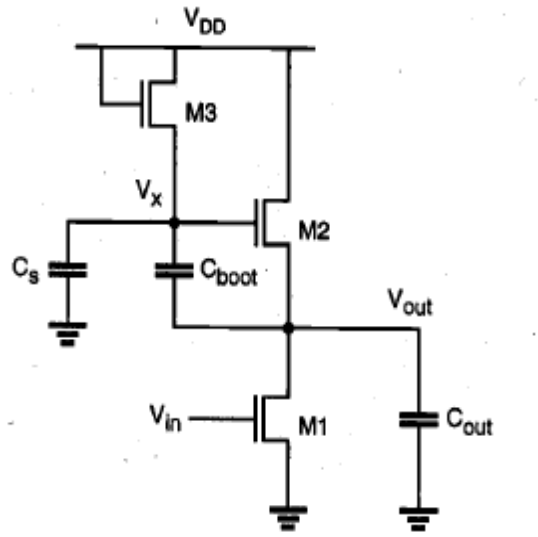


Fig:2. Dynamic bootstrapping arrangement to boost V_x during switching.

Now, assume that the input switches from its logic-high level to 0 V at t = 0. As a result, the driver transistor Ml will turn off and the output voltage V_{out} will start to rise. This change in the output voltage level will now be coupled to V through the bootstrap capacitor, C_{boot} .
Let i_{Cboot} represent the transient current flowing through the capacitor C_{boot} during this charge-up event, and let i_{Cs} be the current through C_s. Assuming that the two current components are approximately equal, we obtain

$$i_{Cs} \approx i_{Cboot} \Leftrightarrow C_S \frac{dV_x}{dt} \approx C_{boot} \frac{d(V_{out} - V_x)}{dt}$$

$$(C_S + C_{boot}) \frac{dV_x}{dt} \approx C_{boot} \frac{dV_{out}}{dt}$$

$$\frac{dV_x}{dt} \approx \frac{C_{boot}}{(C_S + C_{boot})} \cdot \frac{dV_{out}}{dt}$$

$$\int_{V_{DD}-V_{T3}}^{V_x} dV_x = \frac{C_{boot}}{(C_S + C_{boot})} \cdot \int_{V_{OL}}^{V_{DD}} dV_{out}$$

$$V_x = (V_{DD} - V_{T3}) + \frac{C_{boot}}{(C_S + C_{boot})} (V_{DD} - V_{OL})$$

$$V_x(max) = 2V_{DD} - V_{T3} - V_{OL}$$

$$V_x(min) = V_{DD} + V_{T2}\big|_{V_{out}=V_{DD}}$$
$$= \left(V_{DD} - V_{T3}(V_x)\right) + \frac{C_{boot}}{(C_S + C_{boot})}(V_{DD} - V_{OL})$$

$$\frac{C_{boot}}{(C_S + C_{boot})} = \frac{V_{T2}\big|_{V_{out}=V_{DD}} + V_{T3}\big|_{V_x}}{(V_{DD} - V_{OL})}$$

$$\frac{C_{boot}}{C_S} = \frac{V_{T2}\big|_{V_{out}=V_{DD}} + V_{T3}\big|_{V_x}}{V_{DD} - V_{OL} - V_{T2}\big|_{V_{out}=V_{DD}} - V_{T3}\big|_{V_x}}$$

Q.7: What do you mean by ratioed and ratioless logic in synchronous dynamic logic design?
ANS:

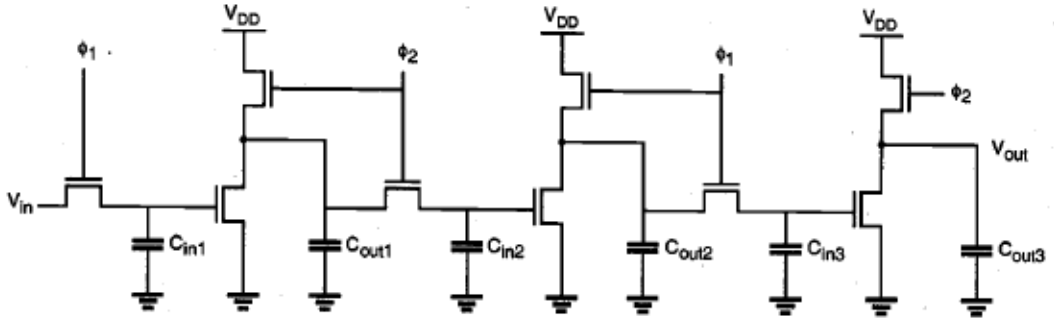


Figure 1. Enhancement-load dynamic shift register (ratioed logic).

In this circuit, the valid low-output voltage level VOL of each stage is strictly determined by the driver-to-load ratio, since the output pass transistor (input pass transistor of next stage) turns on in phase with the load transistor. Therefore, this circuit arrangement is also called **ratioed dynamic logic.**

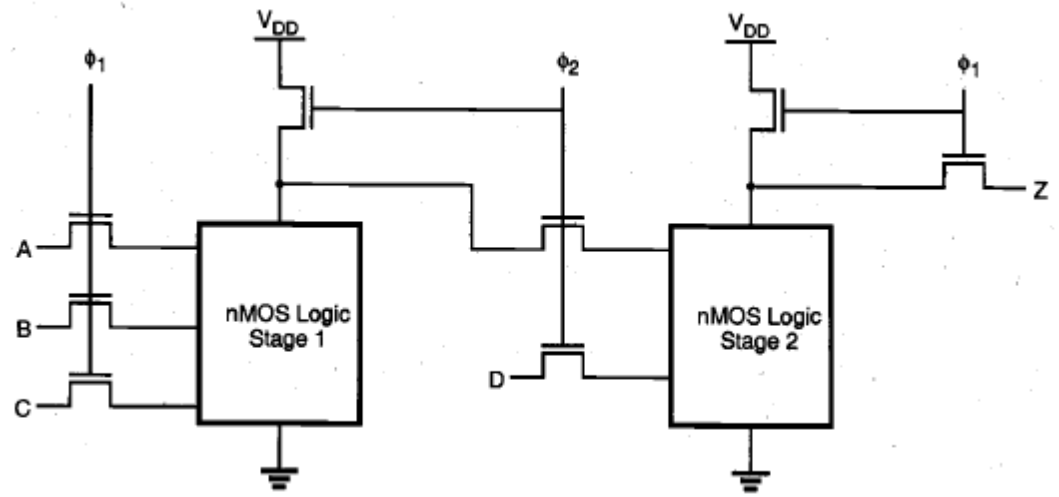


Figure 2. General circuit structure of ratioed synchronous dynamic logic.

When clock Φ_1, becomes active again, the valid output level across C_{out2} is determined and transferred into C_{in3}. Also, a new input level can be accepted into C_{in1}, during this phase. Since the valid logic-low level of $V_{OL} = 0$ V can be achieved regardless of the driver-to-load ratio, this circuit arrangement is called **ratioless dynamic logic**

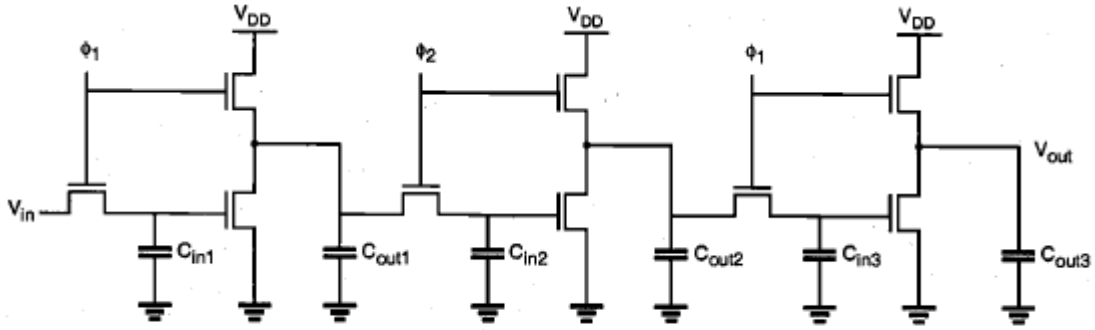


Figure 3. Enhancement-load dynamic shift register (ratioless logic).

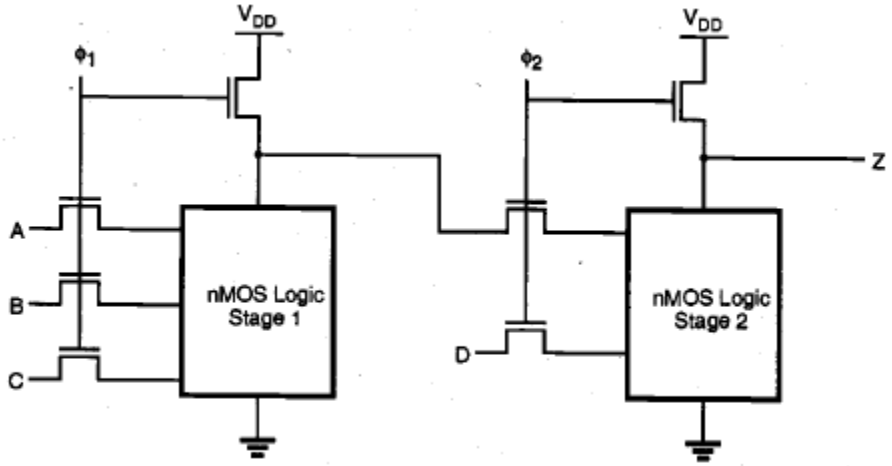
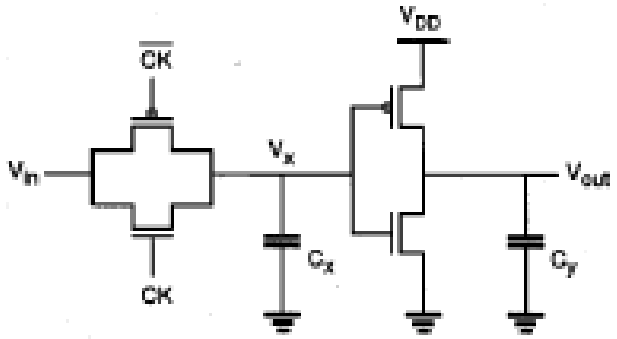


Figure 4. General circuit structure of ratioless synchronous dynamic logic.

Q-8: Draw the basic building block of CMOS Transmission gate dynamic shift register.
ANS:



Q-9:Explain the dynamic CMOS precharge and evaluate state.

ANS:

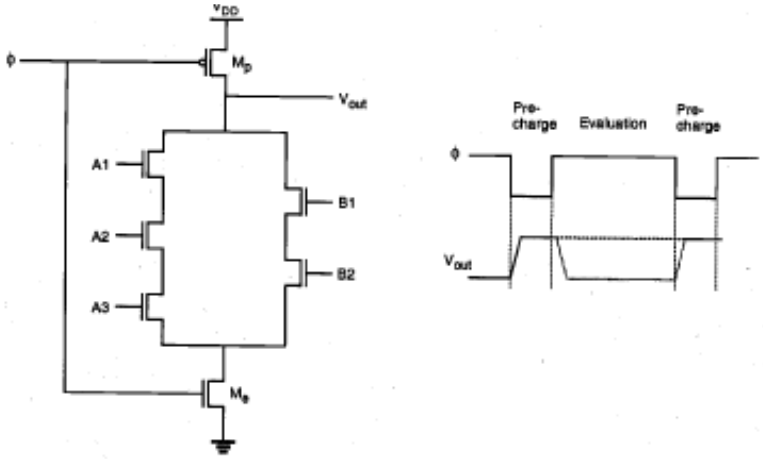


Fig:1. Dynamic CMOS logic gate implementing a complex Boolean function.

A dynamic CMOS circuit technique which allows us to significantly reduce the number of transistors used to implement any logic function. The circuit operation is based on first precharging the output node capacitance and subsequently, evaluating the output level according to the applied inputs. Both of these operations are scheduled by a single clock signal, which drives one nMOS and one pMOS transistor in each dynamic stage. A dynamic CMOS logic gate which implements the function F = $\overline{(A1A2A3 + B1B2)}$ is shown in Fig. 1

When the clock signal is low (precharge phase), the pMOS precharge transistor MP is conducting, while the complementary nMOS transistor M_e is off. The parasitic output capacitance of the circuit is charged up through the conducting pMOS transistor to a logic-high level of $V_{out} = V_{DD}$. The input voltages are also applied during this phase, but they have no influence yet upon the output level since Me is turned off. When the clock signal becomes high (evaluate phase), the precharge transistor M turns off and Me turns on. The output node voltage may now remain at the logic- high level or drop to a logic low, depending on the input

voltage levels. If the input signals create a conducting path between the output node and the ground, the output capacitance will discharge toward V_{OL} = 0 V. The final discharged output level depends on the time span of the evaluation phase. Otherwise, V_{OUT} remains at V_{DD}.

Q11: Explain the cascading problem of Dynamic CMOS logic.
ANS:
For practical multi-stage applications, however, the dynamic CMOS gate presents a significant problem. To examine this fundamental limitation, consider the two-stage cascaded structure shown in Fig. 9.27. Here, the output of the first dynamic CMOS stage drives one of the inputs of the second dynamic CMOS stage, which is assumed to be a two input NAND gate for simplicity.

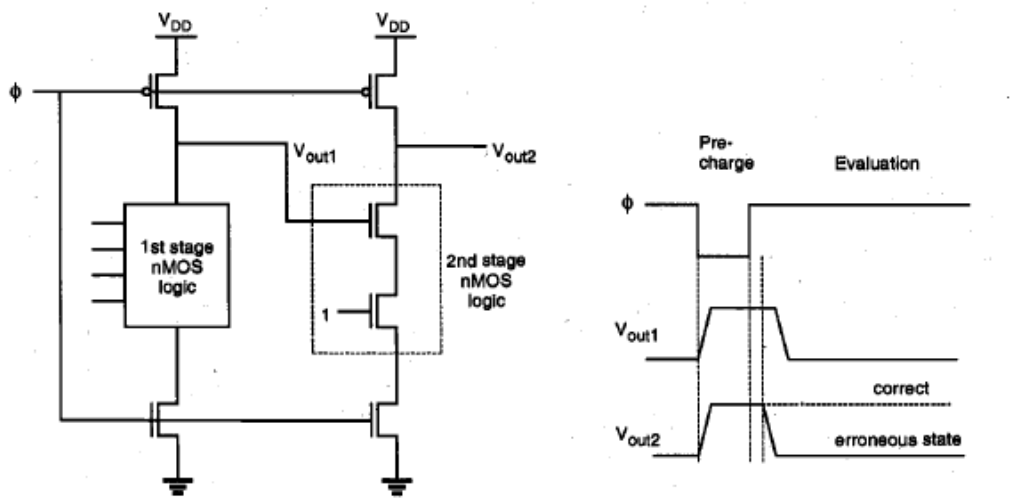


Figure 9.27. Illustration of the cascading problem in dynamic CMOS logic.

During the precharge phase, both output voltages V_{OUT2} and V_{OUT1} are pulled up by the respective pMOS precharge devices. Also, the external inputs are applied during this phase. The input variables of the first stage are assumed to be such that the output V_{OUT1}will drop to logic "0" during the evaluation phase. On the other hand, the external input of the second-stage NAND2 gate is assumed to be a logic " 1," as shown in Fig. 1. When the evaluation phase begins, both output voltages V_{OUT1} and V_{OUT2} are logic-high. The output of the first stage (V_{OUT1}) eventually

drops to its correct logic level after a certain time delay. However, since the evaluation in the second stage is done concurrently, starting with the high value of V_{OUT1} at the beginning of the evaluation phase, the output voltage V_{OUT2} at the end of the evaluation phase will be erroneously low. Although the first stage output subsequently assumes its correct output value once the stored charge is drained, the correction of the second-stage output is not possible. This example illustrates that dynamic CMOS logic stages driven by the same clock signal cannot be cascaded directly. This severe limitation seems to undermine all the other advantages of dynamic CMOS logic, such as low power dissipation, large noise margins, and low transistor count. Alternative clocking schemes and circuit structures must be developed to overcome this problem.

Q-12: What is Domino CMOS logic? Explain its operation.

ANS: A dynamic CMOS logic stage, such as the one shown in Fig. 1, is cascaded with
a static CMOS inverter stage. The addition of the inverter allows us to operate a number of such structures in cascade, as explained in the following.

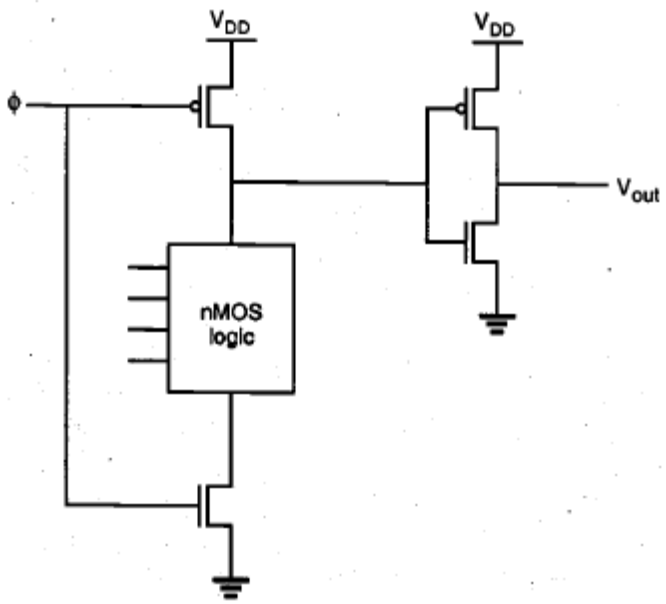


Figure 1 :Generalized circuit diagram of a domino CMOS logic gate.

During the precharge phase (when CK = 0), the output node of the dynamic CMOS stage is precharged to a high logic level, and the output of the CMOS inverter (buffer) becomes low. When the clock signal rises at the beginning of the evaluation phase, there are two possibilities: The output node of the dynamic CMOS stage is either discharged to a low level through the nMOS circuitry (1 to 0

transition), or it remains high. Consequently, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1. Regardless of the input voltages applied to the dynamic CMOS stage, it is not possible for the buffer output to make a 1 to 0 transition during the evaluation phase.

Q13: Draw the CMOS Logic and Domino CMOS logic for the complex logic function :

Z=AB+(C+E)(D+F)+GH

ANS:

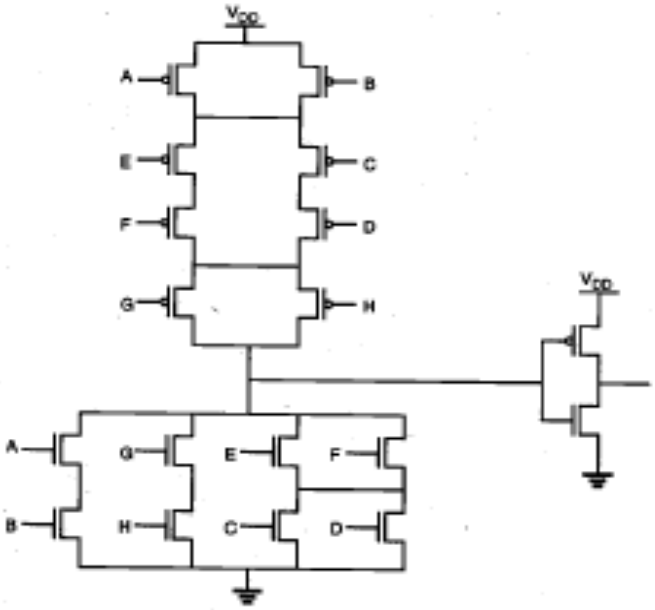


Fig1: CMOS Logic implementation

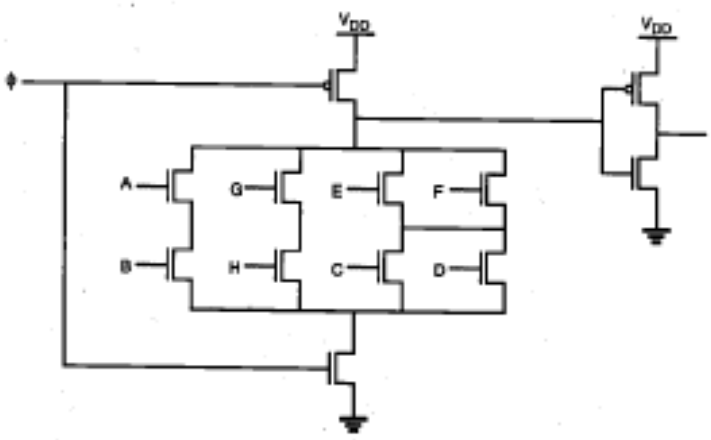


Fig2: Domino Logic implementation

Q-14. What are the advantages and disadvantages of dynamic logic over static logic?

Ans:

- Advantages over static logic:
  - Avoids duplicating logic twice as both N-tree and P-tree, as in standard CMOS
  - Typically can be used in very high performance applications
  - Very simple sequential memory circuits; amenable to synchronous logic
  - High density achievable
  - Consumes less power (in some cases)
- Disadvantages compared to static logic:
  - Problems with clock synchronization and timing
  - Design is more difficult

PET-5H002 DIGITAL VLSI DESIGN

Module-1

Chapter-9: Design for Testability

MULTIPLE CHOICE QUESTIONS:

1. Stuck open (off) fault occur/s due to _____
   a. Excessive variations in fabrication process
   b. Large separation of drain or source diffusion from the gate
   c. Both a and b
   d. None of the above

2. Built-in self test aims to
   a) reduce test pattern generation cost
   b) reduce volume of test data
   c) reduce test time
   d) all of the mentioned

3. The disadvantages of scan based techniques are:

   a) It removes hazards
   b) The testing time increases
   c) uses more complex latches, flip flops , I/O pins
   d) Both b & c

4. _____ technique is used in BIST .

   a) BILBO
   b) I_{DDQ}
   c) LFSR
   d) None

5. LFSR consists of _____
   a) NOT gates
   b) AND gates
   c) EX-OR gates
   d) OR gates

6. For n-bit LFSR, the longest possible sequence is given by
   a) $2^n - 1$
   b) $2^n + 1$
   c) 2^n
   d) n-1

7. Signature analysis performs
   a) addition

b) multiplication
c) amplifies
d) polynomial division

8. Practical guidelines for testability aims at
a) facilitating test generation
b) facilitating test application
c) avoiding timing problems
d) all of the mentioned

9. I_{DDQ} fault occurs when there is
a) increased quiescent current
b) increased voltage
c) increased power supply
d) increased discharge

10) For a circuit with k lines, ____ single stuck-at -fault is possible
a) k
b) 2k
c) k/2
d) k^2

11. Which are processing faults?
a) missing contact window
b) parasitic transistor
c) oxide breakdown
d) all of the mentioned

12. The design technique helps in improving
a) controllability
b) observability
c) controllability and observability
d) overall performance

13) The scan path shift register is verified by
a) shifting in all zeroes first
b) shifting in all ones first
c) adding all ones
d) adding all zeroes

14) In level sensitive process, when the input changes, the response is
a) independent of wiring delays
b) dependent on wiring delays
c) dependent of components
d) independent of input combinations

15) The storage elements in test mode are connected as,
a) parallel shift registers
b) buffers

c) combiners
d) serial shift register

16) In test pattern generation the efficiency is improved by
a) adding buffers
b) partitioning
c) adding multipliers
d) adding power dividers

17) _____ produces Test patterns having both high and least toggle rates.

a) random pattern generator
b) counters
c) LFSR
d) CA

18) High fault coverage can be prevented by
a) fault limit property
b) clock fault property
c) linear interloading property
d) linear dependencies property

19) _____ method is easiest to test.
a) LFSR
b) Counter
c) CA
d) Weighted LFSR

20) The method that does not have carry out is
a) LFSR
b) Counters
c) CA
d) Random sequence generator

21) Accumulators are build with flip flops and _____
a) adders
b) multipliers
c) buffers
d) AND gates

22) The N+M bit test pattern generator has _____ different patterns produced
a) $2^{(N+M)}$
b) $2^{N}+M$
c) $2N^{M}$
d) 2^{M+N}

23) Which process is used to develop LFSR method?
a) bernoulli method
b) scan based method
c) deterministic method
d) Indeterministic method

24) Preloading different starting value for the LFSR is called as
a) seeding
b) reseeding
c) deseeding
d) pre-seeding

25) Primitive polynomial should have minimum number of zero coefficient.
a) true
b) false

26) In testability, which terminology is used to represent or indicate the formal evidences of correctness?
a. Validation
b. Verification
c. Simulation
d. Integration

27) Which among the following is regarded as an electrical fault?
a. Excessive steady-state currents
b. Delay faults
c. Bridging faults
d. Logical stuck-at-0 or stuck-at-1

28) Stuck open (off) fault occur/s due to _____
a. An incomplete contact (open) of source to drain node
b. Large separation of drain or source diffusion from the gate
c. Both a and b
d. None of the above

29) Why is multiple stuck-at fault model preferred for DUT?

a. Because single stuck-at fault model is independent of design style & technology
b. Because single stuck-at tests cover major % of multiple stuck-at faults & unmodeled physical defects
c. Because complexity of test generation is reduced to greater extent in multiple stuck-at fault models
d. All of the above

30) Basically, an observability of an internal circuit node is a degree to which one can observe that node at the _____ of an integrated circuit.
a. Inputs
b. Outputs
c. Both a and b
d. None of the above

Answer key:

1(b), 2(d), 3(d), 4(c), 5(c), 6(a), 7(d), 8(d), 9(a), 10(b), 11(d), 12(c), 13(b), 14(a), 15(d), 16(b), 17(b), 18(d), 19(a), 20(b), 21(a), 22(b), 23(a),24(b), 25(a), 26(b), 27(a),28(c),29(d),30(b)

SUBJECTIVE TYPE QUESTIONS:

1. Write short note on: Stuck at '0' and stuck at '1' faults?

Ans:

- Stuck at faults occur when a line is permanently stuck to Vdd or ground giving a faulty output. This line may be an input or output to any gate. Also this fault can be single or multiple stuck at faults.
- When a signal, or gate output, is stuck at a 0 or 1 value, independent of the inputs to the circuit, the signal is said to be “stuck at” and the fault model used to describe this type error is called a “stuck at fault model”.
- A fault model is an engineering model of something that could go wrong in the construction or operation of a piece of equipment. From the model, the designer or user can then predict the consequences of this particular fault.
- Basic fault models in digital circuits include the stuck-at fault model, the bridging fault model, the transistor faults, the open fault model, the delay fault model, etc. In the past several decades, the most popular fault model used in practice is the single stuck-at fault model.
- To use this fault model, each input pin on each gate in turn, is assumed to be grounded, and a test vector is developed to indicate the circuit is faulty. Hence, if a circuit has n signal lines, there are potentially 2n stuck-at faults defined on the circuit.
- The test vector is a collection of bits to apply to the circuit's inputs, and a collection of bits expected at the circuit's output. If the gate pin under consideration is grounded, and this test vector is applied to the circuit, at least one of the output bits will not agree with the corresponding output bit in the test vector.
- After obtaining the test vectors for grounded pins, each pin is connected in turn to a logic one and another set of test vectors is used to find faults occurring under these conditions. Each of these faults is called a single stuck-at-0 or a singlestuck-at-1 fault, respectively.
- The stuck-at fault model is a logical fault model because no delay information is associated with the fault definition.
- It is also called a permanent fault model because the faulty effect is assumed to be permanent, in contrast to intermittent faults which occur (seemingly) at random and transient faults which occur sporadically, perhaps depending on operating conditions like temperature, power supply voltage or on the data values (high or low voltage states) on surrounding signal lines. The single stuck-at fault model is structural because it is defined based on a structural gate-level circuit model.
- A pattern set with 100% stuck-at fault coverage consists of tests to detect every possible stuck-at fault in a circuit. 100% stuck-at fault coverage does not necessarily guarantee high quality, since

faults of many other kinds—such as bridging faults, opens faults, and transition or delay faults—often occur.

2. What are the different types of faults available in VLSI technology with example?

Ans: Physical defects include:

* Defects in silicon substrate
* Photolithographic defects
* Mask contamination and scratches
* Process variations and abnormalities
* Oxide defects

The electrical faults include:

* Shorts (bridging faults)
* Opens
* Transistor stuck-on, stuck-open
* Resistive shorts and opens
* Excessive change in threshold voltage
* Excessive steady-state currents

The logical faults include:

* Logical stuck-at-0 or stuck-at-I
* Slower transition (delay fault)
* AND-bridging, OR-bridging

An example of NOR2 gate with all faults is given below

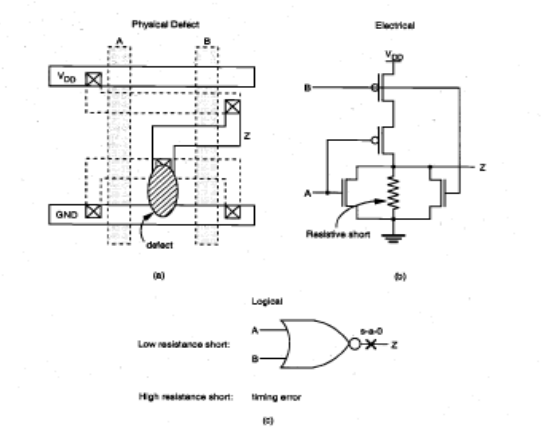


Fig: (a) Physical defects (b) Electrical faults (c) Logical faults

3. Explain the Scan based techniques?

Ans: Scan based techniques is used for the testing of a sequential circuit is reduced to the problem of testing a combinational circuit. A sequential circuit consists of a combinational circuit and some storage elements. In the scan-based design, the storage elements are connected to form a long serial shift register, the so-called scan path, by using multiplexors and a mode (test/normal) control signal. In the test mode, the scan-in signal is clocked into the scan path, and the output of the last stage latch is scanned out. In the normal mode, the scan-in path is disabled and the circuit functions as a sequential circuit. The testing sequence is as follows:

Step 1: Set the mode to test and, let latches accept data from scan-in input,
Step 2: Verify the scan path by shifting in and out the test data.
Step 3: Scan in (shift in) the desired state vector into the shift register.
Step 4: Apply the test pattern to the primary input pins.

Step 5: Set the mode to normal and observe the primary outputs of the circuit after sufficient time for propagation.

Step 6: Assert the circuit clock, for one machine cycle to capture the outputs of the combinational logic into the registers.

Step 7: Return to test mode; scan out the contents of the registers, and at the same time scan in the next pattern.

Step 8: Repeat steps 3-7 until all test patterns are applied.

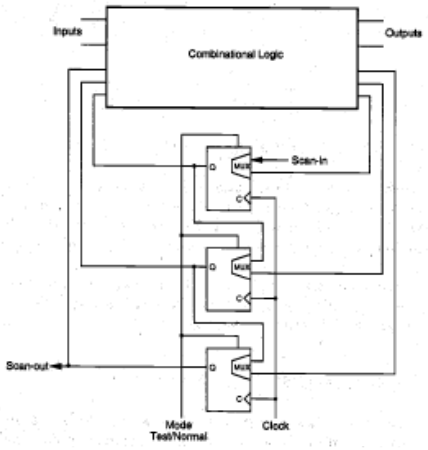


Fig: The general structure of scan-based design.

- The storage cells in scan design can be implemented using edge-triggered D flipflops, master-slave flip-flops, or level-sensitive latches controlled by complementary clock signals to ensure race-free operation.
- In large high-speed circuits, optimizing a single clock signal for skews, etc., both for normal operation and for shift operation, is difficult.
- To overcome this difficulty, two separate clocks, one for normal operation and one for shift operation, are used. Since the shift operation does not have to be performed at the target speed, its clock is much less constrained.
- An important approach among scan-based designs is the level sensitive scan design (LSSD), which incorporates both the level sensitivity and the scan path approach using shift registers.
- The level sensitivity is to ensure that the sequential circuit response is independent of the transient characteristics of the circuit, such as the component and wire delays.
- Thus, LSSD removes hazards and races. Its ATPG is also simplified since tests have to be generated only for the combinational part of the circuit.

4. Describe the Built-in-self-test (BIST) techniques.

Ans:

In built-in self test (BIST) design, parts of the circuit are used to test the circuit itself. Online BIST is used to perform the test under normal operation, whereas off-line BIST is used to perform the test off-line. The essential circuit modules required for BIST include:

* Pseudo random pattern generator (PRPG)
* Output response analyzer (ORA)

The roles of these two modules are illustrated in Fig. The implementation of both PRPG and ORA can be done with Linear Feedback Shift Registers (LFSRs). To test the circuit, test patterns first have to be generated either by using a pseudo random pattern generator, a weighted test generator, an adaptive test generator, or other means. A pseudo random test generator circuit can use an LFSR

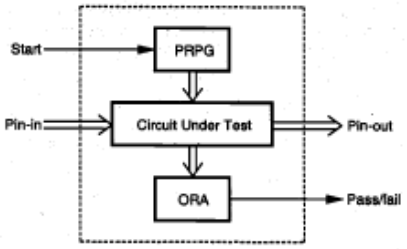


Figure (a) A procedure for BIST.

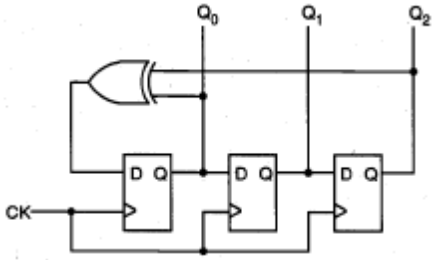


Figure (b) A pseudo-random sequence generator using LFSR.

5. How a linear feedback shift register is used for signature analysis?

Ans:

- The signature analysis, is based on the concept of cyclic redundancy checking. It uses polynomial division, which divides the polynomial representation of the test output data by a characteristic polynomial and then finds the remainder as the signature.
- The signature is then compared with the expected signature to determine whether the device under test is faulty. It is known that compression can cause some loss of fault coverage.
- It is possible that the output of a faulty circuit can match the output of the fault-free circuit; thus, the fault can go undetected in the signature analysis. Such a phenomenon is called aliasing. In its simplest form, the signature generator consists of a single-input linear feedback shift register (LFSR), as shown in Fig (a), in which all the latches are edge-triggered.
- In this case, the signature is the content of this register after the last input bit has been sampled. The input sequence {an) is represented by polynomial G(x) and the output sequence by Q(x).
- It can be shown that
  G(x) = *Q(x) P(x) + R(x),* where P(x) is the characteristic polynomial of LFSR and *R(x)* is the remainder, the degree of which is lower than that of *P(x).* For the simple case in Fig. 16.13, the characteristic polynomial is

$$P(x) = 1 + x^2 + x^4 + x^5$$

For the 8-bit input sequence { 1 1 1 1 0 1 0 1, the corresponding input polynomial is

$$G(x) = x^7 + x^6 + x^5 + x^4 + x^2 + 1$$

and the remainder term becomes *R(x) = x4* + x2, which corresponds to the register contents of {0 0 1 0 1}.

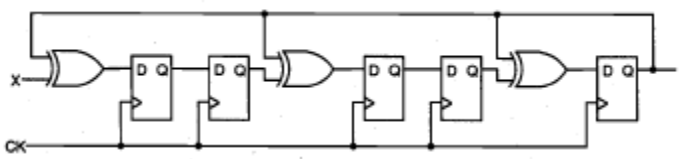


Figure :Polynomial division using LFSR for signature analysis.

6. Write short notes on Current Monitoring I_{DDQ}?

Ans:

The I_{DDQ} test consists of applying the test vector and then monitoring the current drawn from the power supply rail in DC steady state. Although this test requires more testing time, the fault detection capability is greatly improved with small circuit overhead required to monitor the I_{DDQ} in various parts of DUT. While stuck-at tests require both fault sensitization and fault effect propagation, the I_{DDQ} test requires only fault sensitization. However, its performance in open drain and open gate test is less effective. The I_{DDQ} fault coverage is relatively easy to obtain and may potentially offer a full-chip coverage capability for large designs.

The design guidelines for I_{DDQ} testability are as follows:

* Low static current states, e.g., full CMOS is preferred
* No active pull-ups or pull-downs
* No internal drive conflicts, e.g., drivers share a bus
* No floating nodes in the circuit
* No degraded voltages, e.g., must have $V_{OH} = V_{DD}$ and $V_{OL} = 0$

7. What is Built-In Logic Block Observer circuit?

Ans:

The built-in logic block observer (BILBO) register is a form of ORA which can be used in each cluster of partitioned registers. A basic BILBO circuit is shown in Fig. below which allows four different modes controlled by C0 and Cl signals. The BILBO operation allows monitoring of circuit operation through exclusive-ORing into LFSR at multiple points, which corresponds to the signature analyzer with multiple inputs.

C_0	C_1	Mode
0	0	Linear shift
0	1	Reset
1	0	Signature analysis
1	1	Data(complemented) latch

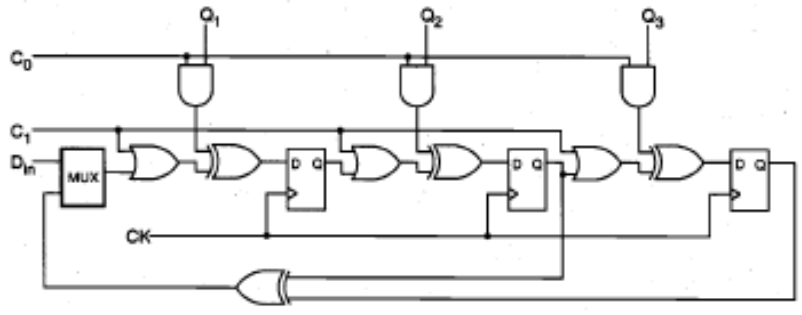


Fig: An example of BILBO

8. How the process of current monitoring I_{DDQ} is used to detect the faults in Fabrication techniques?

Ans:

For testing fabrication defects is the IDDQ test. Under a bridging fault, the static currents drawn from the power supply in CMOS circuits can be noticeably high, well beyond the expected range of leakage currents. For example, if the drain node of the pMOS transistor in a CMOS inverter is

shorted to the power supply rail due to a bridging fault, its IDDQ current can be very high even when the input is high. It can also detect other fabrication defects not easily detected by other test methods, including:

* Gate oxide short
* Channel punch-through
* P-N diode leakage
* Transmission-gate defect

The IDDQ test consists of applying the test vector and then monitoring the current drawn from the power supply rail in DC steady state. Although this test requires more testing time, the fault detection capability is greatly improved with small circuit overhead required to monitor the IDDQ in various parts of DUT.

9. What are the design guidelines of I_{DDQ}?

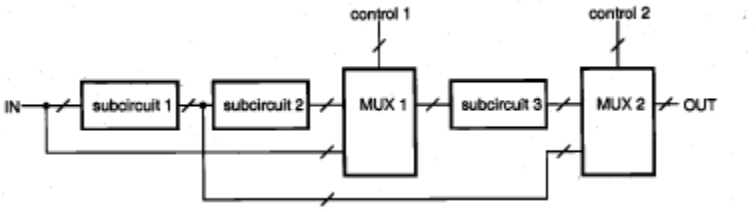
Ans:

* Low static current states, e.g., full CMOS is preferred
* No active pull-ups or pull-downs
* No internal drive conflicts, e.g., drivers share a bus
* No floating nodes in the circuit
* No degraded voltages, e.g., must have $V_{OH} = V_{DD}$ and $V_{OL} = 0$

10. Discuss the Partition and Mux technique?

Ans:

Since the sequence of many serial gates, functional blocks, or large circuits are difficult to test, such circuits can be partitioned and multiplexors (muxes) can be inserted such that some of the primary inputs can be fed to partitioned parts through multiplexers with accessible control signals. With this design technique, the number of accessible nodes can be increased and the number of test patterns can be reduced. A case in point would be the 32-bit counter. Dividing this counter into two 16-bit parts would reduce the testing time in principle by a factor of **215.** However, circuit partitioning and addition of multiplexers may increase the chip area and circuit delay. This practice is not unique and is similar to the divide-and-conquer approach to large, complex problems.



11. List the different types of fault models which causes timing failures at target speed?

Ans:

The different types of fault models which causes timing failures at target speed

* Improper estimation of on-chip interconnect delays and other timing considerations,
* Excessive variations in the fabrication process which cause significant variations in circuit delays and clock skews,
* Opens in metal lines connecting parallel transistors which make the effective transistor size much smaller,
* Aging effects such as hot-carrier induced delay increase.