LECTURE NOTES

ON

MICROPROCESSOR & MICROCONTROLLER

(INTERFACING DEVICES)

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8255A (Programmable Peripheral Interface)

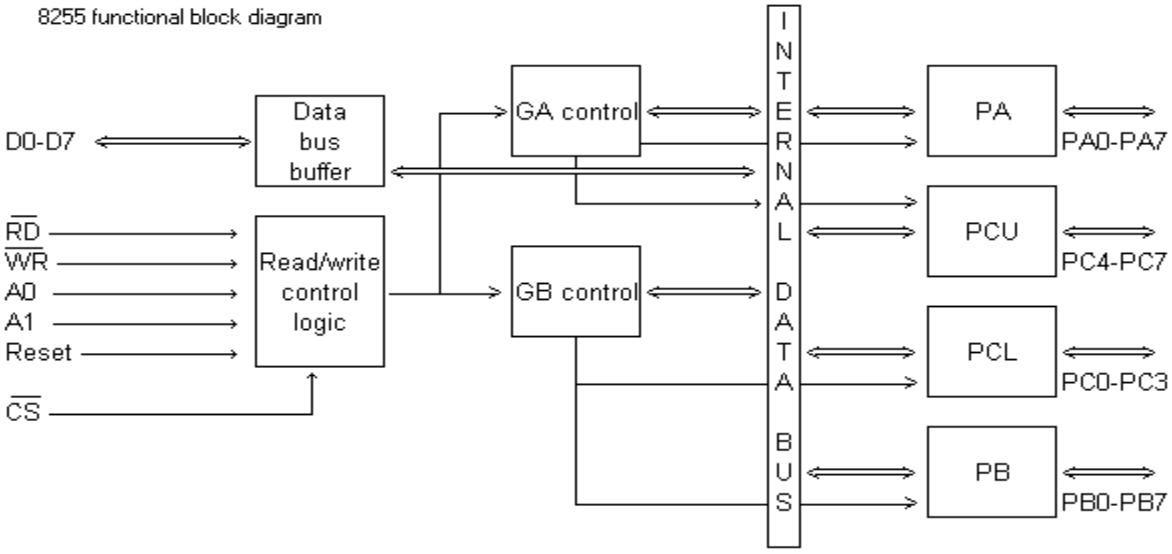
Introduction

The Intel 8255A is a widely used general purpose programmable I/O device designed for use with Intel microprocessor. This PPI implements a general purpose I/O interface to connect peripheral equipment to a microcontroller system bus. The core's functional configuration is programmed by the system software so that external logic is not required to interface the peripheral device. It has 24 I/O pins which can be programmed as single bit,4-bits and byte wide input and output ports. It is a widely used PPI due to its simple, versatile and economical features.

Features

- 40 pins IC designed by CMOS technology.
- Among 40 pins , 24 pins are used for I/O operation. They can be grouped into two 8-bit parallel ports (port A, port B) and remaining 8 pins for port C. Port C can also be used as port C upper (PC_u) and port C lower (PC_l) each of 4-bits.
- All ports can be programmed to act as input port or output port or both by writing the control word in the control register.
- Three programming modes (mode 0, mode 1, mode 2) for all ports and bit set reset (BSR) mode for port C.
- 8-bit bidirectional system data bus with standard microprocessor interface.
- Compatible with almost all Intel family.
- Used to interface the keyboard and parallel printer in many micro controller system.

Block diagram of 8255A



(Block diagram of 8255)

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Over these lines, commands, status information and data are transferred between MPU and 8255A, whenever MPU

Read/Write control logic

The function of this block is to manage all the internal and external transfers of both data and control or status words. It accepts inputs from the CPU address and control busses and in turn, issues commands to the both of control groups.

It has six lines. The functions are as follows:

- RD(Read): It enables the read operation. When this signal is low, the MPU reads data from a selected I/O port through data bus from 8255A.

- WR(write): A ‘low’ on this input pin enables the CPU to write data or control words in the selected I/O or in the control register.

- RESET(Reset) : This active high signal clears the control; register and set all the ports in the input mode.

- CS(chip select) : A ‘low’ on this input pin enables the communication between the 8255A and the MPU.

- A0 and A1: these input signals are used to select one of the three ports or the control register.

A0	**A1**	**Selected**
0	0	Port A

0	1	Port B
1	0	Port C
1	1	CR (control Register)

Group A and Group B controls

The functional configuration of each port is programmed by the system software. In essence, the VCPU 'outputs' a control word to the 8255A. The control word contains information such mode 'bit set', 'bit reset' etc., which initializes the functional configuration of 8255A.

Each of the control blocks (Group A and Group B) accepts commands from the read/write command logic , receives the 'control words' from the internal data bus and issues the proper commands to its associated ports.

Control Group A→ Port A and Port C upper (PCu)

Control Group B → Port B and Port C lower (PCl)

The control word register can only be written into, no read operation of the control word register is allowed.

Port A, B and C

The 8255A contains three 8-bit ports (A ,B and C). All can be configured in a wide verity of functional characteristics by the system software but each has its own special features to further enhance the power and flexibility of the 8255A.

- Port A : One 8-bit data output latch/ buffer and one 8-bit data input latch.
- port B : One 8-bit data input/ output latch/ buffer and one 8-bit data input buffer.
- Port C: One 8-bit data output latch/buffer and one 8-bit data input buffer. This p[ort can be divided into two 4-bit port under the mode control.

Pin description

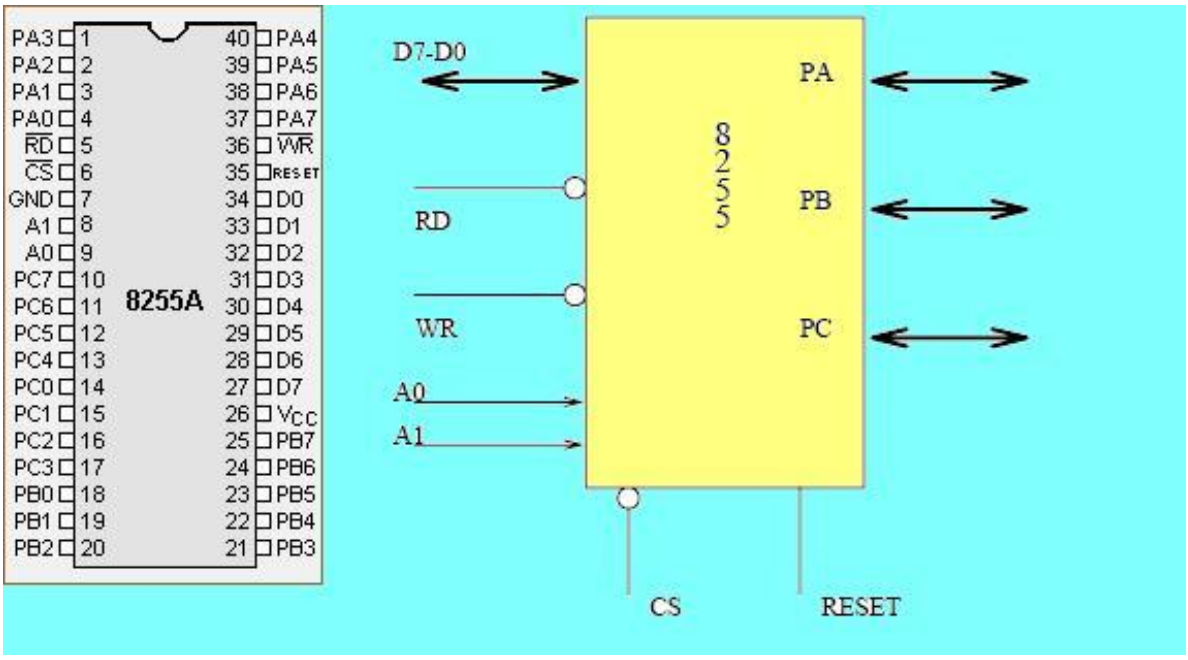


Fig 4.2 (Pin diagram of 8255)

Pin	Description
$D_0 - D_7$	Data lines
RESET	Reset input
$\overline{CS}$	Chip select
$\overline{RD}$	Read control
$\overline{WR}$	Write control
A_0, A_1	Internal address
$PA_7 - PA_0$	Port-A pins
$PB_7 - PB_0$	Port-B pins
$PC_7 - PC_0$	Port-C pins
V_{CC}	+5V
V_{SS}	0V (GND)

(Description of pins in 8255)

Operating modes of 8255A

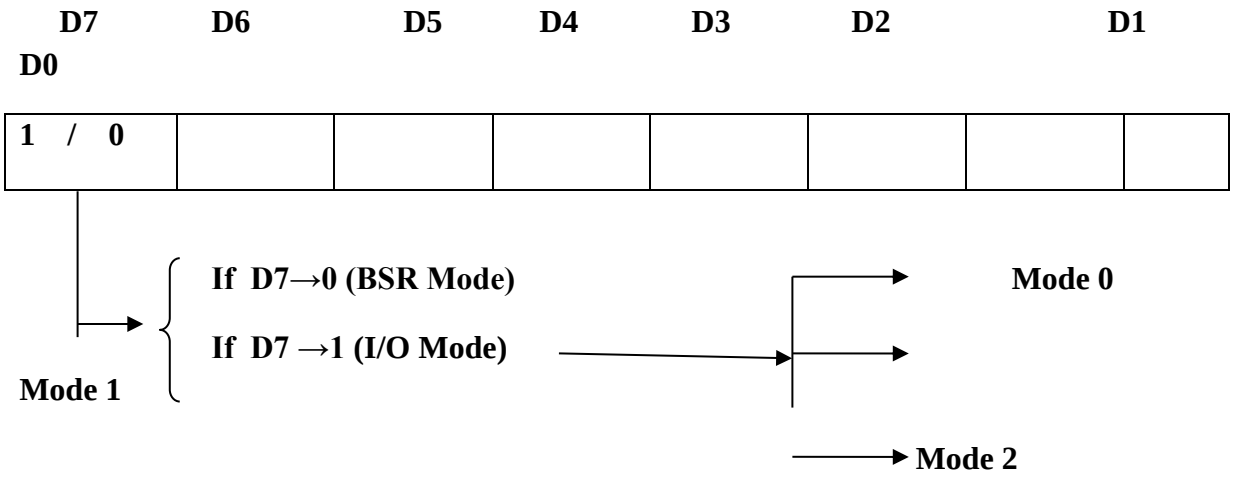
When the reset pin goes 'high', all the ports are set to the input mode (i.e, all 24 pins will be in the high impedance state). After the reset is removed the 8255A remains in the input mode.

The 8255A is having a control register (8-bit). The content of the register is called control word, which specifies the I/O operation for each port.

The MSB(D7) of the control register decides the two possible modes of operation, BSR mode and I/O mode.

Again I/O mode is divided into three different modes, Mode 0, Mode 1, and Mode 2.

CONTROL REGISTER



(Mode selection by control register)

I/O Mode

Mode 0 Operation

This functional configuration provides simple input and output operation for each of three ports. No handshaking signals are exchanged, data are simply written to or read from a specified port.

Mode 0 basic functional definition

- Two 8-bit ports and two 4-bit ports
- Any port can be input or output
- Output are latched
- Input are not latched
- 16 different I/O configurations are possible in this mode.

Mode 1 Operation

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or handshaking signals. In Mode 1, Port A and Port B uses the lines on port C to generate or accept the handshaking signals.

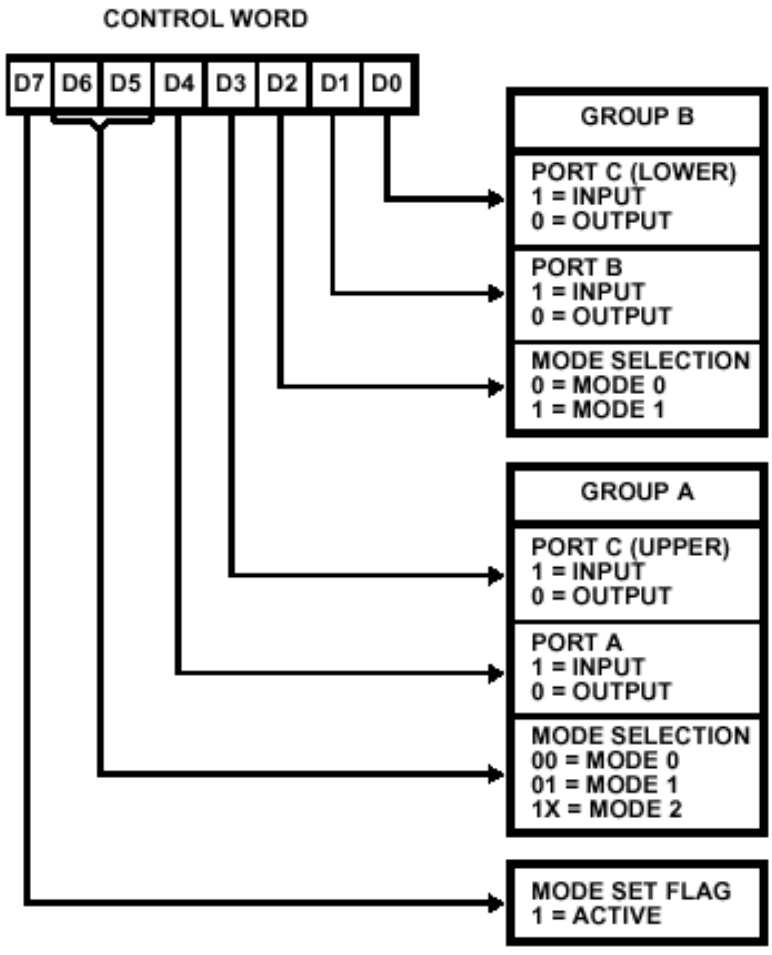
Mode 1 Basic Functional Definitions

- Two groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control port.
- When port B used as a I/O port , then PC0,PC1,PC2 are used for handshaking or control.
- When Port A used as I/P port , then PC3,PC4,PC5 are used for controlling and when port A used as O/P port ,then PC3,PC6,PC7 are used for controlling.
- The combination of Mode 0 and Mode 1 is also possible.

Mode 2 operation

This functional configuration provides a mean for communicating with a peripheral device on a single 8-bit bus for both transmitting and receiving the data. Handshaking signal are provide to maintain proper data flow in a similar manner as in mode 1.

Mode 2 basic functional definition



- Applicable for Port A only.
- When port A is used for mode 2 operation then PC3 to PC7 are used for controlling and at that time port is used either in mode 0 or in mode 1operation.
- It is otherwise called as strobe bidirectional mode.

CONTROL WORD FORMAT FOR I/O MODE

Fig 4.5 (Bit pattern of control register in I/O mode)

COMMUNICATION WITH THE PERIPHERAL THROUGH 8255

→ Identify the port address using A0, A1 and CS

→ Determine the control word according to the above format given.

→ Write I/O instructions to communicate with peripherals through ports.

Calculation of Port address

Memory mapped I/O

Assuming the 16-bit address, A15 is the chip select line (high) and all don't care lines are at logic 0, the port address are as follows.

Address **A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0**

Port A 1 0 0 0 0 0 0 0 0 0 0 0 0 0 **0** **0** - 8000H

Port B 1 0 0 0 0 0 0 0 0 0 0 0 0 0 **0** **1** - 8001H

Port C 1 0 0 0 0 0 0 0 0 0 0 0 0 0 **1** **0** - 8002H

CR 1 0 0 0 0 0 0 0 0 0 0 0 0 0 **1** **1** - 8003H

A1 and A0 have been taken as port selection

Peripheral or I/O mapped I/O

Assuming the 8-bit address, A7 is the chip select line (high) and all don't care lines are at logic 0, the port address are as follows.

Address **A7 A6 A5 A4 A3 A2 A1 A0**

Port A 1 0 0 0 0 0 0 0→80H

Port B 1 0 0 0 0 0 0 1→81H

Port C 1 0 0 0 0 0 1 0→82H

CR 1 0 0 0 0 0 1 1→83H

A1 and A0 have been taken as port selection

Example

Write the control word for 8255 operated in mode 0 and specifications are PA-I/P, PB-O/P, PCu-I/P, and PCl -O/P.

Ans:

D7 D6 D5 D4 D3 D2 D1 D0

1	**0**	**0**	**1**	**1**	**0**	**0**	**0**

Control word= 98H

Example

Write the control word for 8255 operated in mode 1 and specifications are PA-O/P, PB-O/P, PC4 & PC5-I/P.

Ans:

D7	D6	D5	D4	D3	D2	D1	D0
1	**0**	**1**	**0**	**1**	**1**	**0**	**x**

Control word= ACH OR ADH

Example

Write the control word for 8255 operated in mode 1 and specifications are PA- Bidirectional mode 2, PB- mode 0 & I/P, PC0, PC1 & PC2-O/P.

Ans:

D7	D6	D5	D4	D3	D2	D1	D0
1	**1**	**x**	**x**	**x**	**0**	**1**	**0**

Control word= C2H OR FAH(Taking all **x**'s to zeros or ones)

Example

Suppose switch have been interfaced at port A and LEDs are at port B in peripheral mapped I/O. Write down the program in 8086 assembly language to read data from switches and display at LEDs in mode 0.

Ans:

D7	D6	D5	D4	D3	D2	D1	D0
1	**0**	**0**	**1**	**x**	**0**	**1**	**x**

Control word : 90H

Program:
```
MOV AL, 90H
OUT 83H, AL
IN AL, 80H
OUT 81H, AL
```

Example

Suppose a 8255A is configured so that port A is an output port, both port B and C are input port in peripheral mapped I/O. Write down the program that will input the data at port B and C, find the difference (port C-port B), and output this difference in port A in mode 0.

Ans:

D7	D6	D5	D4	D3	D2	D1	D0
1	**0**	**0**	**0**	**1**	**0**	**1**	**1**

Control word: 8BH

Program:

```
MOV AL, 8BH
OUT 83H, AL
IN AL, 81H
MOV BL, AL
IN AL, 82H
SUB AL, BL
OUT 80H, AL
```

Example

Write the sequence of instructions needed to initialize the control register of 8255A, so that the port A is an output port and port B and C are input port in mode) operation. Also write the program that will input the contents of port B and C, AND them together, and output the results to port A in memory mapped I/O scheme.

Ans:

D7	D6	D5	D4	D3	D2	D1	D0
1	**0**	**0**	**1**	**1**	**0**	**1**	**1**

Control word : 8BH

Program: Assuming the segment address is already defined.

```
MOV AL, 8BH
MOV [8003H], AL
MOV AL, [8001H]
MOV BL. [8002H]
```

AND AL, BL
MOV [8000H], AL

BSR mode

It is only applicable for port C and other ports are unaffected.

This becomes operational by resetting the D7 bit of control register.

Any of the eight bits of Port C can be Set or Reset using a single OUT put instruction. This feature reduces software requirements in Control-based applications **.** When Port C is being used as status/control for Port A or B these Bits can be set or reset by just as if they were data output port.

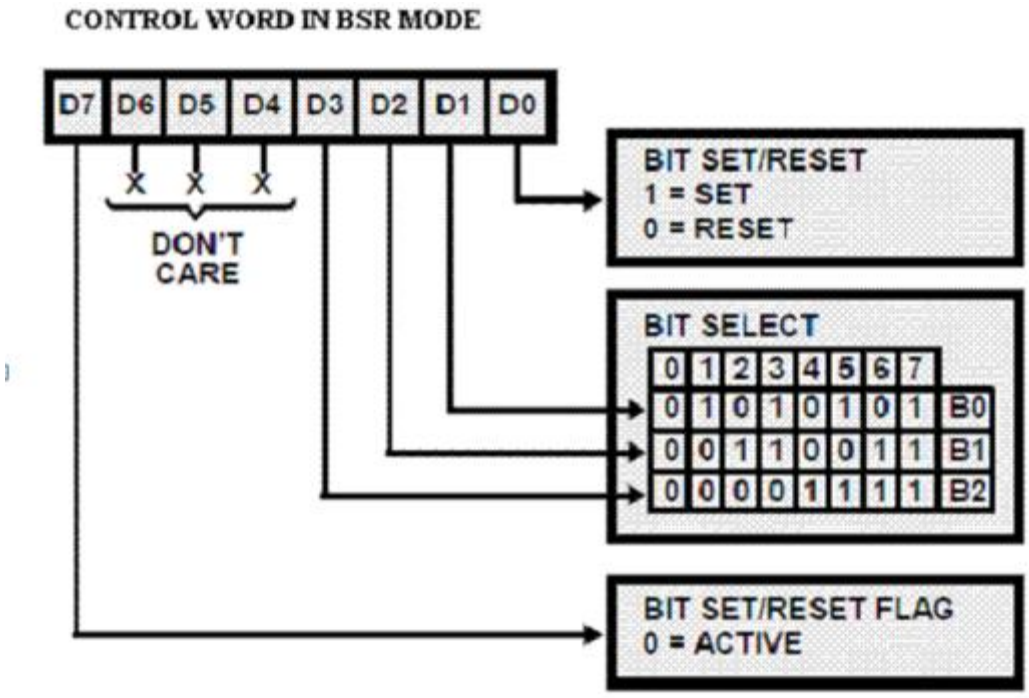


Fig4.6 (Bit pattern in BSR mode)

Example

Write the control word for 8255 operated in BSR mode to set PC7 and to reset PC3.

Ans:

D7 D6 D5 D4 D3 D2 D1 D0

0	**X**	**X**	**x**	**1**	**1**	**1**	**1**

D7	D6	D5	D4	D3	D2	D1	D0
0	**X**	**X**	**x**	**0**	**1**	**1**	**0**

Control word for PC7 : 0FH

Control word for PC3 : 06H

Example

Suppose a switch is connected to d7 bit of port C. Write down a program to toggle the switch at some time delay.

Ans: Control word to set PC7: 0FH and to reset the PC7 : 0EH

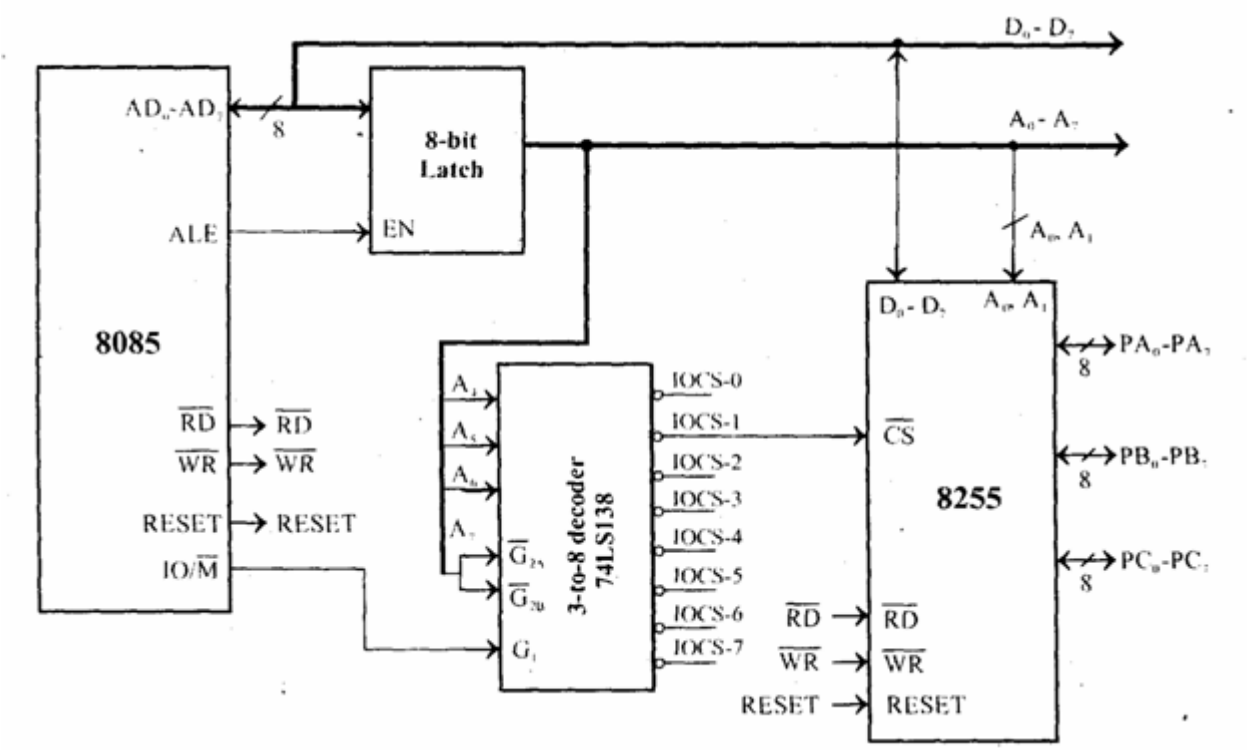
Program:

```
BACK:   MOV AL, 0FH
        OUT 83H, AL
        CALL NEAR PTR XXX
        MOV AL, 0EH
        OUT 82H, ALH
        CALL NEAR PTR XXX
        JMP BACK

XXX:  MOV CL, Count
L1:   NOP
      DEC CL
      JN Z L1
      RET
```

INTERFACING OF 8255

Interfacing of 8255 with 8085 processor:



8237(DMA CONTROLLER)

Basic DMA operation

• The direct memory access (DMA) I/O technique provides direct access to the memory while the microprocessor is temporarily disabled.
• A DMA controller temporarily borrows the address bus, data bus, and control bus from the microprocessor and transfers the data bytes directly between an I/O port and a series of memory location.
• The DMA transfer is also used to do high-speed memory-to-memory transfers.
• Two control signals are used to request and acknowledge a DMA transfer in the microprocessor-based system.
• The HOLD signal is a bus request signal which asks the microprocessor to release control of the buses after the current bus cycle.
• The HLDA signal is a bus grant signal which indicates that the microprocessor has indeed released control of its buses by placing the buses at their high-impedance states.
• The HOLD input has a higher priority than the INTR or NMI interrupt pins.

Features of 8237

• The 8237A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The 8237A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

• The 8237A is designed to be used in conjunction with an external 8-bit address latch. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips. The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to autoinitialize to its original condition following an End of Process (EOP). Each channel has a full 64K address and word count capability.

• The 8237 DMA controller supplies the memory and I/O with control signals and memory address information during the DMA transfer.

• The 8237 is a four-channel device that is compatible to the 8086/8088 microprocessors and can be expanded to include any number of DMA channel inputs.

• The 8237 is capable of DMA transfers at rates of up to 1.6M bytes per second.

• Each channel is capable of addressing a full 64K-byte section of memory and can transfer up to 64K bytes with a single programming.

Block diagram

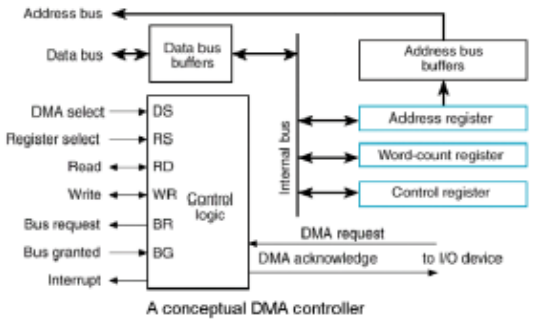
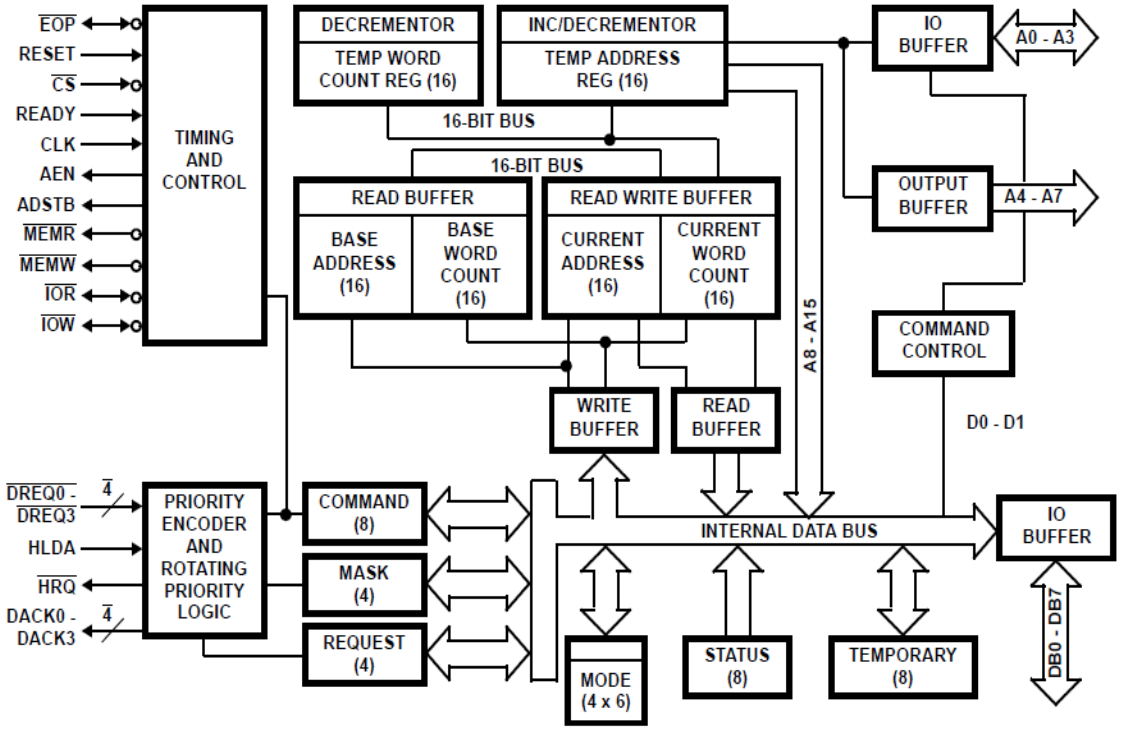


Fig 5.1 (a) and (b)



The above diagram is showing the detail block diagram of 8237 and the explanation of each block is given in the in the section 5.4 and 5.5.

PIN DIAGRAM OF 8237

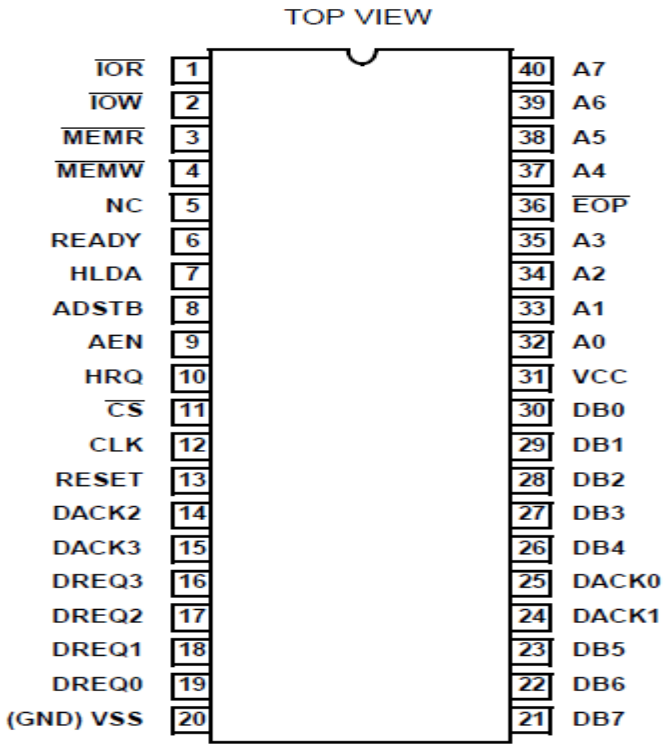


Fig 5.2 (Pin diagram of 8237)

VCC: Power (a 5V supply)

VSS: Ground.

CLK: Clock Input controls the internal operations of the 8237A and its rate of data transfers. The input may be driven at up to 5 MHz for the 8237A-5.

CS (CHIP SELECT): Chip Select is an active low input used to select the 8237A as an I/O device during the Idle cycle. This allows CPU communication on the data bus.

RESET: Reset is an active high input which clears the Command, Status, Request and Temporary registers. It also clears the first/ last flip/flop and sets the Mask register. Following a Reset the device is in the Idle cycle.

READY: Ready is an input used to extend the memory read and write pulses from the 8237A to accommodate slow memories or I/O peripheral devices. Ready must not make transitions during its specified setup/hold time.

HLDA (HOLD ACKNOWLEDGE): The active high Hold Acknowledge from the CPU indicates that it has relinquished control of the system busses.

DREQ0-DREQ3 (DMA REQUEST): The DMA Request lines are individual asynchronous channel request inputs used by peripheral circuits to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. A request is generated by activating the DREQ line of a channel. DACK will acknowledge the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be maintained until the corresponding DACK goes active.

DB0-DB7 (DATA BUS): The Data Bus lines are bidirectional three-state signals connected to the system data bus. The outputs are enabled in the Program condition during the I/O Read to output the contents of an Address register, a Status register, the Temporary register or a Word Count register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the 8237A control registers.

During DMA cycles the most significant 8 bits of the address are output onto the data bus to be strobe into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the 8237A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs place the data into the new memory location.

IOR (I/O READ): I/O Read is a bidirectional active low three-state line . In the Idle cycle, it is an input control signal used by the CPU to read the control registers. In the Active cycle, it is an output control signal used by the 8237A to access data from a peripheral during a DMA Write transfer.

IOW (I/O WRITE): I/O Write is a bidirectional active low three-state line. In the Idle cycle, it is an input control signal used by the CPU to load information into the 8237A. In the Active cycle, it is an output control signal used by the 8237A to load data to the peripheral during a DMA Read transfer.

EOP (END OF PROCESS): End of Process (EOP) is an active low bidirectional signal. Information concerning the completion of DMA services is available at the bidirectional EOP pin.

The 82C37A allows an external signal to terminate an active DMA service by pulling the EOP pin low. A pulse is generated by the 82C37A when terminal count (TC) for any channel is reached, except for channel 0 in memory-to-memory mode. During memory-to-memory transfers, EOP will be output when the TC for channel 1 occurs.

The EOP pin is driven by an open drain transistor on-chip, and requires an external pull-up resistor to VCC.

When an EOP pulse occurs, whether internally or externally generated, the 82C37A will terminate the service, and if autoinitialize is enabled, the base registers will be written to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by EOP unless the channel is programmed for autoinitialize. In that case, the mask bit remains clear.

A0-A3 (ADDRESS): The four least significant address lines are bidirectional three-state signals. In the Idle cycle they are inputs and are used by the CPU to address the register to be loaded or read. In the Active cycle they are outputs and provide the lower 4 bits of the output address.

A4-A7 (ADDRESS): The four most significant address lines are three-state outputs and provide 4 bits of address. These lines are enabled only during the DMA service.

HRQ (HOLD REQUEST): This is the Hold Request to the CPU and is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes 8237A to issue the HRQ.

DACK0-DACK3 (DMA ACKNOWLEDGE): DMA Acknowledge is used to notify the individual peripherals when one has been granted a DMA cycle. The sense of these lines is programmable. Reset initializes them
to active low.

AEN (ADDRESS ENABLE): Address Enable enables the 8-bit latch containing the upper 8 address bits onto the system address bus. AEN can also be used to disable other system bus drivers during DMA transfers. AEN is active HIGH.

ADSTB (ADDRESS STROBE): This is an active high signal used to control latching of the upper address byte. It will drive directly the strobe input of external transparent octal latches, such as the 82C82. During block operations, ADSTB will only be issued when the upper address byte must be updated, thus speeding operation through elimination of S1 states. ADSTB timing is referenced to the falling edge of the 82C37A clock.

MEMR (MEMORY READ): The Memory Read signal is an active low three state output used to access data from the selected memory location during a DMA Read or a memory-to-memory transfer.

MEMW (MEMORY WRITE): The Memory Write is an active low three-state output used to write data to the selected memory location during a DMA Write or a memory-to-memory transfer.

NC (NO CONNECT): Pin 5 is open**.**

Internal register

NAME	SIZE	NUMBER
Base Address Registers	16-Bits	4
Base Word Count Registers	16-Bits	4
Current Address Registers	6-Bits	4
Current Word Count Registers	16-Bits	4
Temporary Address Register	16-Bits	1
Temporary Word Count Register	16-Bits	1
Status Register	8-Bits	1
Command Register	8-Bits	1
Temporary Register	8-Bits	1
Mode Registers	6-Bits	4
Mask Register	4-Bits	1
Request Register	4-Bits	1

Table 5.1 (list of register in 8237)

Current Address Register - Each channel has a 16-bit Current Address register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented by one after each transfer and the values of the address are stored in the Current Address register during the transfer. This register is written or read by the microprocessor in successive 8-bit bytes.
It may also be reinitialized by an autoinitialize back to its original value. Autoinitialize takes place only after an EOP.

Current Word Count Register - Each channel has a 16-bit Current Word Count register. This register determines the number of transfers to be performed. The actual number of transfers will be one more than the number programmed in the Current Word Count register (i.e., programming a count of 100 will result in 101 transfers). The word count is decremented after each transfer. When the value in the register goes from zero to FFFFH, a TC will be generated. This register is loaded or read in successive 8-bit bytes by the microprocessor in the Program Condition. Following the end of a DMA service it may also be reinitialized by an autoinitialization back to its original value. Autoinitialization can occur only when an EOP occurs. If it is not autoinitialized, this register will have a count of FFFFH after TC.

Base Address and Base Word Count Registers – Each channel has a pair of Base Address and Base Word Count registers. These 16-bit registers store the original value of their associated current registers. During autoinitialize these values are used to restore the current registers to their original values. The base registers are written simultaneously with

their corresponding current register in 8- bit bytes in the Program Condition by the microprocessor. These registers cannot be read by the microprocessor.

Note: writing a value to the base address register automatically loads the same value in the current address register because initially the current address register points to the starting I/O or memory address. To load the a new 16-bit address into the base register, two separate byte must be written, one after another, to the address of the register. The 82C37A has an internal flip-flop called the first/last flip-flop. This flip-flop identifies which byte of the address is being written into the register. If the flip-flop is logic 0 then low byte is accessed and for logic 1 high byte. For example, to write the address 6789H into the base address register and the current word register for channel 0 of a DMAC located at the base address NEXT, then the following instructions may be executed.

```
MOV AL, 89H
OUT NEXT+0, AL
MOV AL, 67H
OUT NEXT+0, AL (+0 is used for channel 0)
```

Similarly the count register can be programmed in the same way as just described for the address register. For example to program a count of OFFFH into the base and current count registers for channel 1 of a DMAC located at address NEXT, the following instructions may be executed.

```
MOV AL, FFH
OUT  DMA+3, AL
MOV AL, 0FH
OUT  DMA+3, AL
```

The following table shows the details address of all the register along with the status of flip-flop.

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0–DB7
			$\overline{CS}$	$\overline{IOR}$	$\overline{IOW}$	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0–A7
			0	1	0	0	0	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0–A7
			0	0	1	0	0	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0–W7
			0	1	0	0	0	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0–W7
			0	0	1	0	0	0	1	1	W8–W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0–A7
			0	1	0	0	0	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0–A7
			0	0	1	0	0	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0–W7
			0	1	0	0	0	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0–W7
			0	0	1	0	0	1	1	1	W8–W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0–A7
			0	1	0	0	1	0	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0–A7
			0	0	1	0	1	0	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0–W7
			0	1	0	0	1	0	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0–W7
			0	0	1	0	1	0	1	1	W8–W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0–A7
			0	1	0	0	1	1	0	1	A8–A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0–A7
			0	0	1	0	1	1	0	1	A8–A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0–W7
			0	1	0	0	1	1	1	1	W8–W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0–W7
			0	0	1	0	1	1	1	1	W8–W15

Table 5.2 (Address of register in 8237)

Command Register - This 8-bit register controls the operation of the 82C37A. It is programmed by the microprocessor and is cleared by RESET or a Master Clear instruction. The following diagram lists the function of the Command register bits. See Figure 4 for Read and Write addresses.

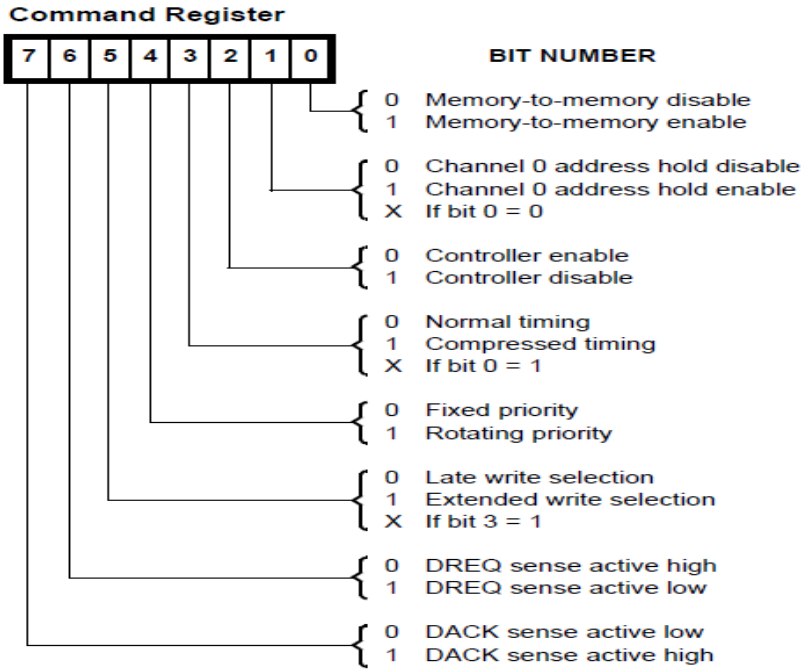


Fig 5.3 (Bit pattern of command register)

Mode Register - Each channel has a 6-bit Mode register associated with it. When the register is being written to by the microprocessor in the Program condition, bits 0 and 1 determine which channel Mode register is to be written. When the processor reads a Mode register, bits 0 and 1 will both be ones. See the following diagram for Mode register functions and addresses.

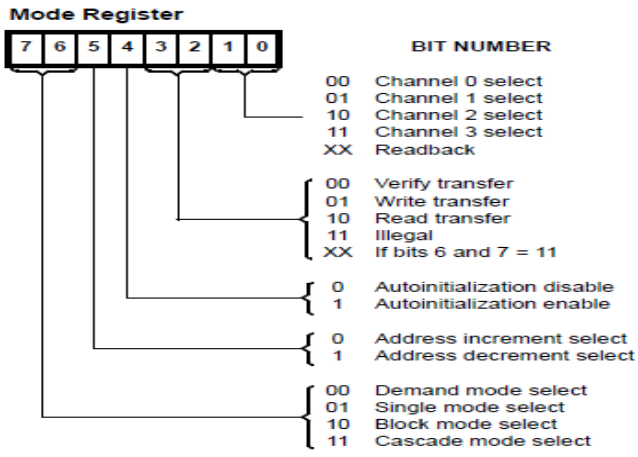


Fig 5.4 (Bit pattern of mode register)

Request Register - The 82C37A can respond to requests for DMA service which are initiated by software as well as by a DREQ. Each channel has a request bit associated with

it in the 4-bit Request register. These are non-mask able and subject to prioritization by the Priority Encoder network. Each register bit is set or reset separately under software control. The entire register is cleared by a Reset or Master Clear instruction. To set or reset a bit, the software loads the proper form of the data word. See Figure for register address coding, and the following diagram for Request register format. A software request for DMA operation can be made in block or single modes. For memory-to-memory transfers, the software request for channel 0 should be set. When reading the Request register, bits 4-7 will always read as ones, and bits 0-3 will display the request bits of channels 0-3 respectively.

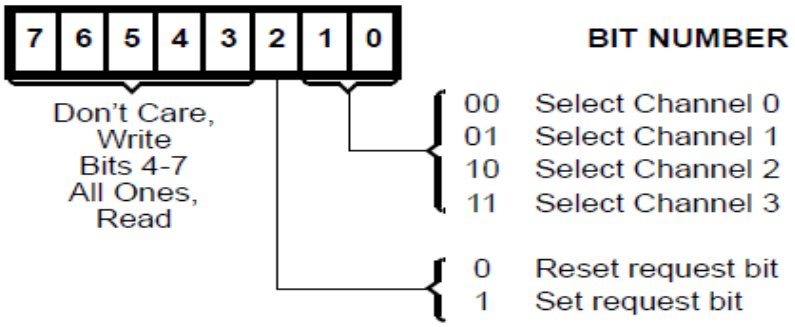


Fig 5.5 (Bit pattern of request register)

Mask Register - Each channel has associated with it a mask bit which can be set to disable an incoming DREQ. Each mask bit is set when its associated channel produces an EOP if the channel is not programmed to Autoinitialize. Each bit of the 4-bit Mask register may also be set or cleared separately or simultaneously under software control. The entire register is also set by a Reset or Master clear. This disables all hardware DMA requests until a Clear Mask Register instruction allows them to occur. The instruction to separately set or clear the mask bits is similar in form to that used with the Request register. Refer to the following diagram and Figure for details. When reading the Mask register, bits 4-7 will always read as logical ones, and bits 0-3 will display the mask bits of channels 0-3, respectively. The 4 bits of the Mask register may be cleared simultaneously by using the Clear Mask Register command.

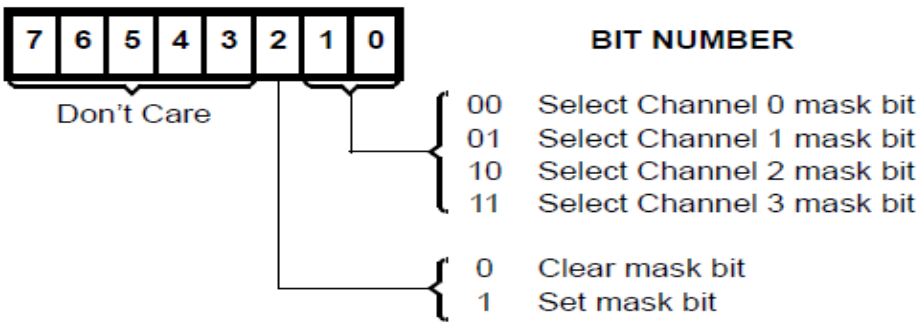


Fig 5.6.a (Bit pattern of mask register)

All 4-bits of mask register may also be written with a single command.

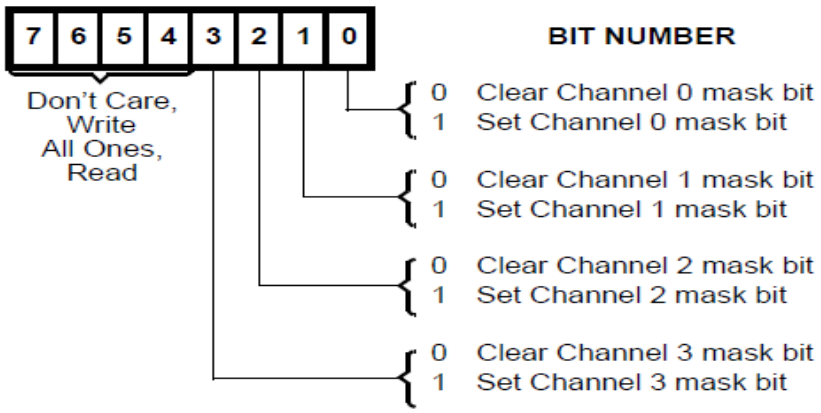


Fig 5.6.b (Bit pattern of mask register)

Status Register - The Status register is available to be read out of the 82C37A by the microprocessor. It contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests. Bits 0-3 are set every time a TC is reached by that channel or an external EOP is applied. These bits are cleared upon RESET, Master Clear, and on each Status Read. Bits 4-7 are set whenever their corresponding channel is requesting service, regardless of the mask bit state. If the mask bits are set, software can poll the Status register to determine which channels have DREQs, and selectively clear a mask bit, thus allowing user defined service priority. Status bits 4-7 are updated while the clock is high, and latched on the falling edge. Status Bits 4-7 are cleared upon RESET or Master Clear.

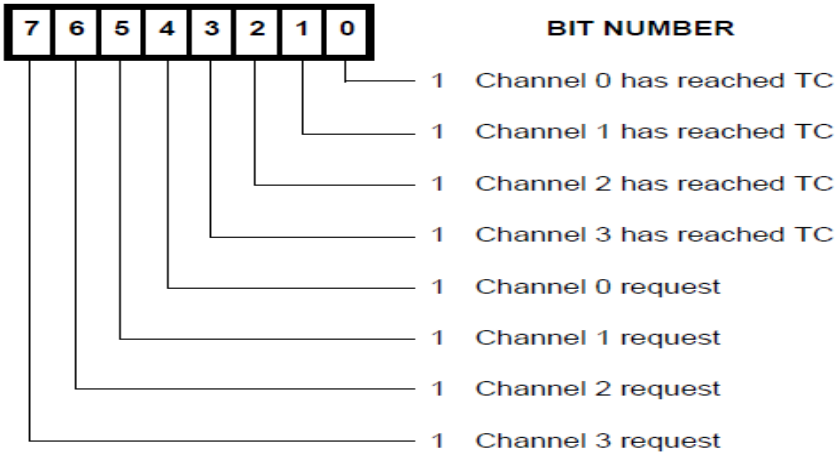


Fig 5.7 (Bit pattern of Status register)

Temporary Register-The Temporary register is used to hold data during memory-to-memory transfers.

Following the completion of the transfers, the last word moved can be read by the microprocessor in the Program Condition. The Temporary register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a Reset.

DMA Operation

In a system, the 82C37A address and control outputs and data bus pins are basically connected in parallel with the system busses. An external latch is required for the upper address byte. While inactive, the controller's outputs are in a high impedance state. When activated by a DMA request and bus control is relinquished by the host, the 82C37A drives the busses and generates the control signals to perform the data transfer. The operation performed by activating one of the four DMA request inputs has previously been programmed into the controller via the Command, Mode, Address, and Word Count registers.

For example, if a block of data is to be transferred from RAM to an I/O device, the starting address of the data is loaded into the 82C37A Current and Base Address registers for a particular channel, and the length of the block is loaded into the channel's Word Count register. The corresponding Mode register is programmed for a memory-to-I/O operation (read transfer), and various options are selected by the Command register and the other Mode register bits. The channel's mask bit is cleared to enable recognition of a DMA request (DREQ). The DREQ can either be a hardware signal or a software command.
Once initiated, the block DMA transfer will proceed as the controller outputs the data address, simultaneous MEMR and IOW pulses, and selects an I/O device via the DMA acknowledge (DACK) outputs. The data byte flows directly from the RAM to the I/O device. After each byte is transferred, the address is automatically incremented (or decremented) and the word count is decremented. The operation is then repeated for the next byte. The controller stops transferring data when the Word Count register underflows, or an external EOP is applied.

DMA Execution

The process of data transfer from the peripheral to the memory under the DMA controller can be classified under two modes: the slave mode and the master mode.

Slave mode: In this 8237 DMAC is initialised, and treated as a peripheral by-

1. MPU selects the DMAC through the chip select.
2. MPU writes the control word in command and mode register.

Master mode:

1. When peripheral is ready for data transfer, it sends a high signal on DRQ of DMAC.
2. Then DMAC sets HRQ to high and ultimately the HOLD pin of microprocessor is enable.
3. The microprocessor relinquishes the busses and sends an acknowledgement signal through HLDA.
4. After receiving the HLDA, the DMAC asserts AEN signal high causes the AD0-AD7 multiplexed bus acts for A0-A7.
5. Then asserts ADSTB high and places the content of data bus (which is higher order address A8-A15of starting address) on A15 to A8 of microprocessor. At the same time DMAC also outputs the low order address A7 to A0 on the A7 to A0 of microprocessor.
6. When the entire the address A15 to A0on address bus, the DMAC sends DACK to the peripheral.
7. The data transfer is taking place by the necessary control signal until DACK remains high.
8. At the end, the DMAC asserts **EOP^** (end of process) signal low to inform the peripheral that all the data has been transferred.

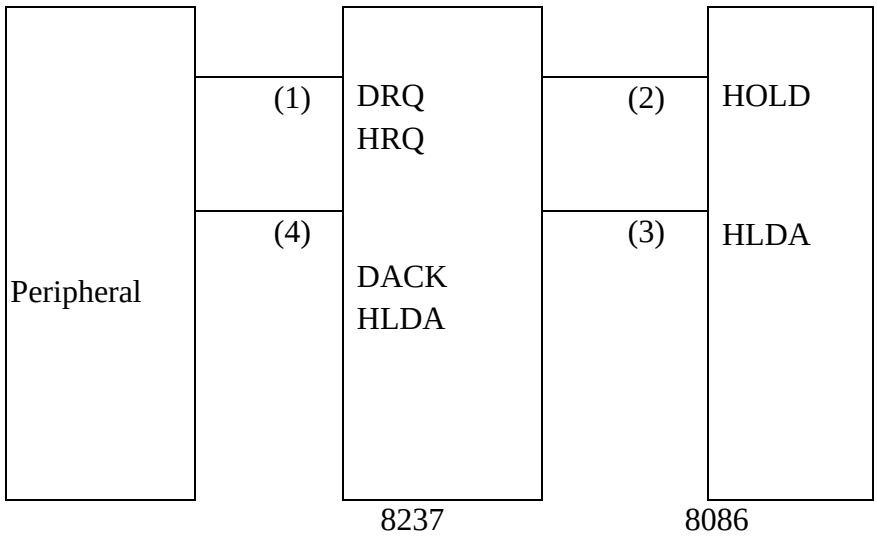


Fig 5.8 (operational procedure in DMA process)

Mode of operation

It is operated in four modes:

Single Transfer Mode - In Single Transfer mode, the device is programmed to make one transfer only. The word count will be decremented and the address decremented or incremented following each transfer. When the word count "rolls over" from zero to FFFFH, a terminal count bit in the status register is set, an EOP pulse is generated, and the channel will autoinitialize if this option has been selected. If not programmed to autoinitialize, the mask bit will be set, along with the TC bit and EOP pulse. DREQ must be held active until DACK becomes active. If DREQ is held active throughout the single transfer, HRQ will go inactive and release the bus to the system. It will again go active and, upon receipt of a new HLDA, another single transfer will be performed, unless a higher priority channel takes over. In 8080A, 8085A, 80C88, or 80C86 systems, this will ensure one full machine cycle execution between DMA transfers. Details of timing between the 82C37A and other bus control protocols will depend upon the characteristics of the microprocessor involved.

Block Transfer Mode - In Block Transfer mode, the device is activated by DREQ or software request and continues making transfers during the service until a TC, caused by word count going to FFFFH, or an external End of Process (EOP) is encountered. DREQ need only be held active until DACK becomes active. Again, an autoinitialization will occur at the end of the service if the channel has been programmed for that option.

Demands Transfer Mode - In Demand Transfer mode the device continues making transfers until a TC or external EOP is encountered, or until DREQ goes inactive. Thus, transfer may continue until the I/O device has exhausted its data capacity After the I/O device has had a chance to catch up, the DMA service is re-established by means of a DREQ. During the time between services when the microprocessor is allowed to operate, the intermediate values of address and word count are stored in the 82C37A Current Address and Current Word Count registers. Higher priority channels may intervene in the demand process, once DREQ has gone inactive. Only an EOP can cause an autoinitialization at the end of service. EOP is generated either by TC or by an external signal.

Cascade Mode - This mode is used to cascade more than one 82C37A for simple system expansion. The HRQ and HLDA signals from the additional 82C37A are connected to the DREQ and DACK signals respectively of a channel for the initial 82C37A.This allows the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is preserved and the new device must wait for its turn to acknowledge requests. Since the cascade channel of the initial 82C37A is used only for prioritizing the additional device, it does not output an address or control signals of its own. These could conflict with the outputs of the active channel in the added device. The initial 82C37A will respond to DREQ and generate DACK but all other outputs except HRQ will be disabled. An external EOP will be ignored by the
initial device, but will have the usual effect on the added device. Figure 3 shows two additional devices cascaded with an initial device using two of the initial device's channels. This forms a two-level DMA system. More 82C37As could be added at the second level by using the remaining channels of the first level. Additional devices can also be added by cascading into the channels of the second level devices, forming a third level.

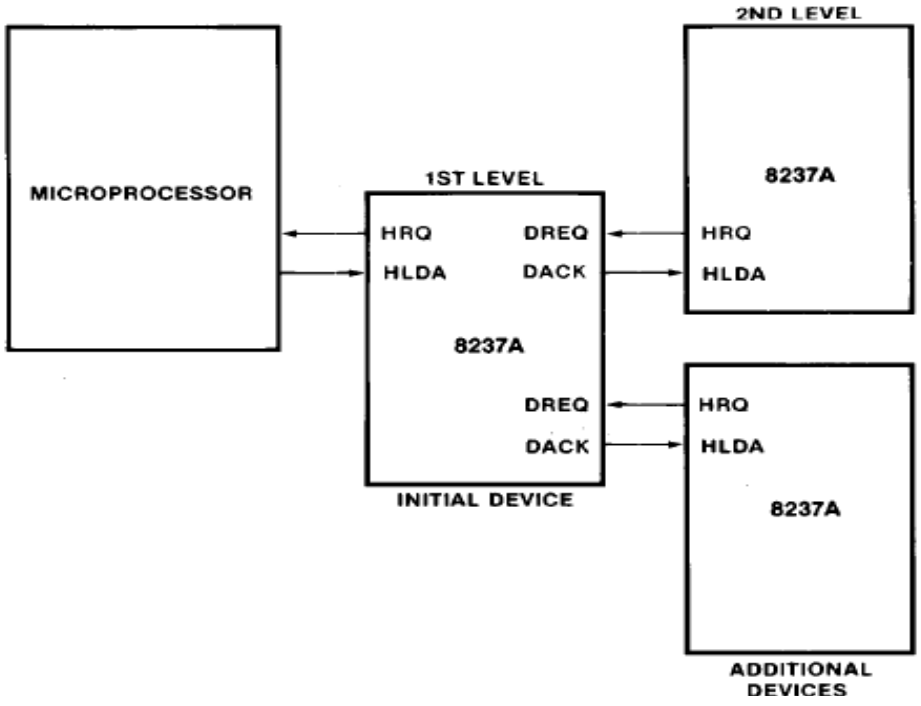


Fig 5.9 (Cascade mode of 8237)

When programming cascaded controllers, start with the first level device (closest to the microprocessor). After RESET, the DACK outputs are programmed to be active low and are held in the high state. If they are used to drive HLDA directly, the second level device(s) cannot be programmed until DACK polarity is selected as active high on the initial device. Also, the initial device's mask bits function normally on cascaded channels, so they may be used to inhibit second level services.

Transfer types

Autoinitialize: By setting bit 4 in the Mode register, a channel may be set up as an autoinitialize channel. During autoinitialization, the original values of the Current Address and Current Word Count registers are automatically restored from the Base Address and Base Word Count registers of the channel following EOP. The base registers are loaded simultaneously with the current registers by the microprocessor and remain unchanged throughout the DMA service. The mask bit is not set when the channel is in autoinitialize mode. Following autoinitialization, the channel is ready to perform another DMA service, without CPU intervention, as soon as a valid DREQ is detected, or software request made.

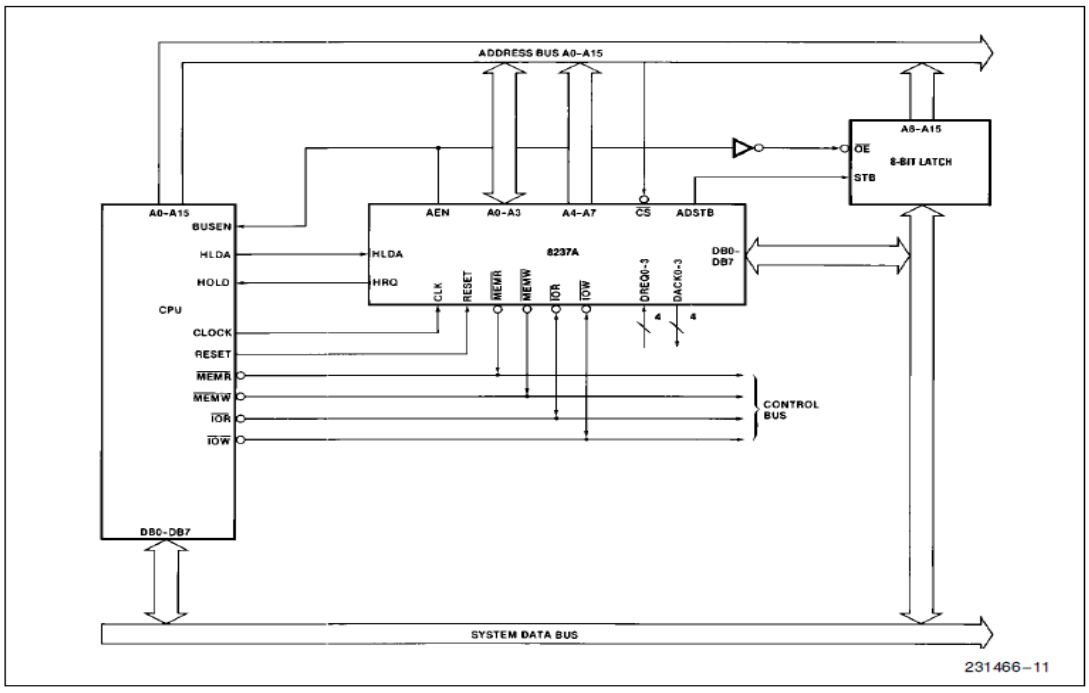
Memory-to-Memory: To perform block moves of data from one memory address space to another with minimum of program effort and time, the 82C37A includes a memory-to-memory transfer feature. Setting bit 0 in the Command register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software or hardware DREQ for channel 0. The 82C37A requests a DMA service in the normal manner. After HLDA is true, the device, using four-state transfers in Block Transfer mode, reads data from the memory. The channel 0 Current Address register is the source for the address used and is decremented or incremented in the normal manner. The data byte read from the memory is stored in the 82C37A internal Temporary register. Another four-state transfer moves the data to memory using the address in channel one's Current Address register and incrementing or decrementing it in the normal manner. The channel 1 Current Word Count is decremented. When the word count of channel 1 decrements to FFFFH, a TC is generated causing an EOP output, terminating the service, and setting the channel 1 TC bit in the Status register. The channel 1 mask bit will also be set, unless the channel 1 mode register is programmed for autoinitialization. Channel 0 word count decrementing to FFFFH will not set the channel 0 TC bit in the status register nor generate an EOP, nor set the channel 0 mask bit in this mode. It will cause an autoinitialization of channel 0, if that option has been selected. If full autoinitialization for a memory-to-memory operation is desired, the channel 0 and channel 1 word counts must be set to equal values before the transfer begins. Otherwise, if channel 0 underflows before channel 1, it will autoinitialize and set the data source address back to the beginning of the block. If the channel 1 word counts underflows before channel 0, the memory-to-memory DMA service will terminate, and channel 1 will autoinitialize but channel 0 will not. In memory-to-memory mode, Channel 0 may be programmed to retain the same address for all transfers. This allows a single byte to be written to a block of memory. This channel 0 address hold feature is selected by setting bit 1 in the Command register. The 82C37A will respond to external EOP signals during memory-to-memory transfers, but will only relinquish the system busses after the transfer is complete (i.e. after an S24 state). It should be noted that an external EOP cannot cause the channel 0 Address and Word Count registers to autoinitialize, even if the Mode register is programmed for autoinitialization. An external EOP will autoinitialize the channel 1 registers, if so programmed. Data comparators in block search schemes may use the EOP input to terminate the service when

a match is found. The timing of memory-to-memory transfers is found in Figure 13. Memory-to-memory operations can be detected as an active AEN with no DACK outputs.

Priority - The 82C37A has two types of priority encoding available as software selectable options. The first is Fixed Priority which fixes the channels in priority order based upon the descending value of their numbers. The channel with the lowest priority is 3 followed by 2, 1 and the highest priority channel, 0. After the recognition of any one channel for service, the other channels are prevented from interfering with the service until it is completed. The second scheme is Rotating Priority. The last channel to get service becomes the lowest priority channel with the others rotating accordingly. The next lower channel from the channel serviced has highest priority on the following request. Priority rotates every time control of the system busses is returned to the processor.

SYSTEM INTERFACE

Figure 5.10 shows a convenient method for configuring a DMA system with the 8237A controller and an 8080A/8085A microprocessor system. The multimode DMA controller issues a HRQ to the processor whenever there is at least one valid DMA request from a peripheral device. When the processor replies with a HLDA signal, the 8237A takes control of the address bus, the data bus and the control bus. The address for the first transfer operation comes out in two bytes the least significant 8 bits on the eight address outputs and the most significant 8 bits on the data bus. The contents of the data bus are then latched into an 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high speed, 8-bit, three-state latch in a 20-pin package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are provided when one 8237A is used.



(System interface)

8254 (Programmable Interval Timer)

Features

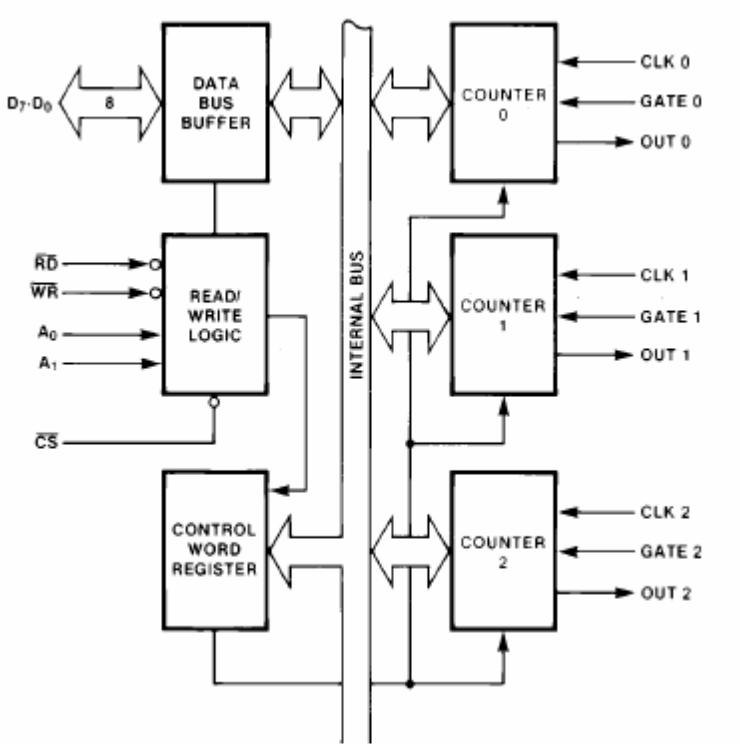
- ✓ Compatible with All Intel and Most other Microprocessors
- ✓ Handles Inputs from DC to 10 MHz 8 MHz 8254 10 MHz 8254-2
- ✓ Status Read-Back Command
- ✓ Six Programmable Counter Modes
- ✓ Three Independent 16-Bit Counters
- ✓ Binary or BCD Counting
- ✓ Single a 5V Supply
- ✓ Standard Temperature Range
- ✓ The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design.
- ✓ It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz .
- ✓ All modes are software programmable. The 8254 is a superset of the 8253.
- ✓ The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.

Functional Description

- ✓ The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems.
- ✓ It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.
- ✓ The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay.
- ✓ After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.
- ✓ Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:

    - ➢ Real time clock
    - ➢ Event-counter
    - ➢ Digital one-shot
    - ➢ Programmable rate generator
    - ➢ Square wave generator

Block Diagram

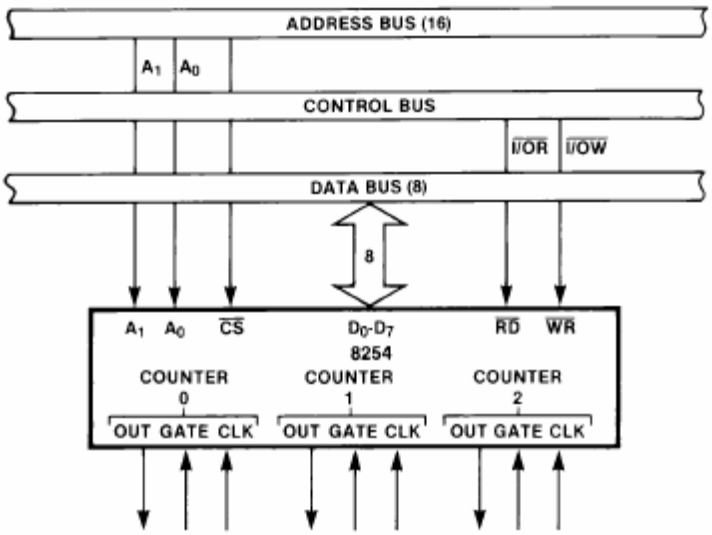


- DATA BUS BUFFER: This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus, see the figure below : Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions.
- READ/WRITE LOGIC: The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 8254. A1 and A0 select one of the three counters or the Control Word Register to be read from/written into.
- A “low” on the RD input tells the 8254 that the CPU is reading one of the counters.
- A ``low'' on the WR input tells the 8254 that the CPU is writing either a Control Word or an initial count. Both RD and WR are qualified by CS; RD and WR are ignored unless the 8254 has been selected by holding CS low.
- **CONTROL WORD REGISTER:** The Control Word Register is selected by the Read/Write Logic when A1,A0 = 11. If the CPU then does a write operation to the 8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.
- The Control Word Register can only be written to; status information is available with the Read-Back Command.
- **COUNTER 0, COUNTER 1, COUNTER 2** :These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

- The Counters are fully independent. Each Counter may operate in a different Mode.
- The Control Word Register is shown in the figure, it is not part of the Counter itself, but its contents determine how the Counter operates.
- The status register, shown in Figure 5, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)
- The actual counter is labelled CE (for ``Counting Element"). It is a 16-bit presettable synchronous down counter. OLM and OLL are two 8-bit latches. OL stands for ``Output Latch"; the subscripts M and L stand for ``Most significant byte" and ``Least significant byte" respectively.
- Both are normally referred to as one unit and called just OL. These latches normally ``follow'' the CE, but if a suitable Counter Latch Command is sent to the 8254, the latches ``latch" the present count until read by the CPU and then return to ``following" the CE.
- One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.
- Similarly, there are two 8-bit registers called CRM and CRL (for ``Count Register"). Both are normally referred to as one unit and called just CR.
- When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously.
- CRM and CRL are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero.
- Note that the CE cannot be written into, whenever a count is written, it is written into the CR.
- The Control Logic is also shown in the diagram.
- CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

8254 SYSTEM INTERFACE: The 8254 is a component of the Intel Microcomputer Systems and interfaces in the same manner as all other peripherals of the family.

- It is treated by the system's software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.
- Basically, the select inputs A0,A1 connect to the A0,A1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.



Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Programming the 8254

- Counters are programmed by writing a Control Word and then an initial count.
- The Control Words are written into the Control Word Register, which is selected when A1, A0 = 11. The Control Word itself specifies which Counter is being programmed.
- **Write Operations**: The programming procedure for the 8254 is very flexible. Only two conventions need to be remembered:

  1) For each Counter, the Control Word must be written before the initial count is written.

2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

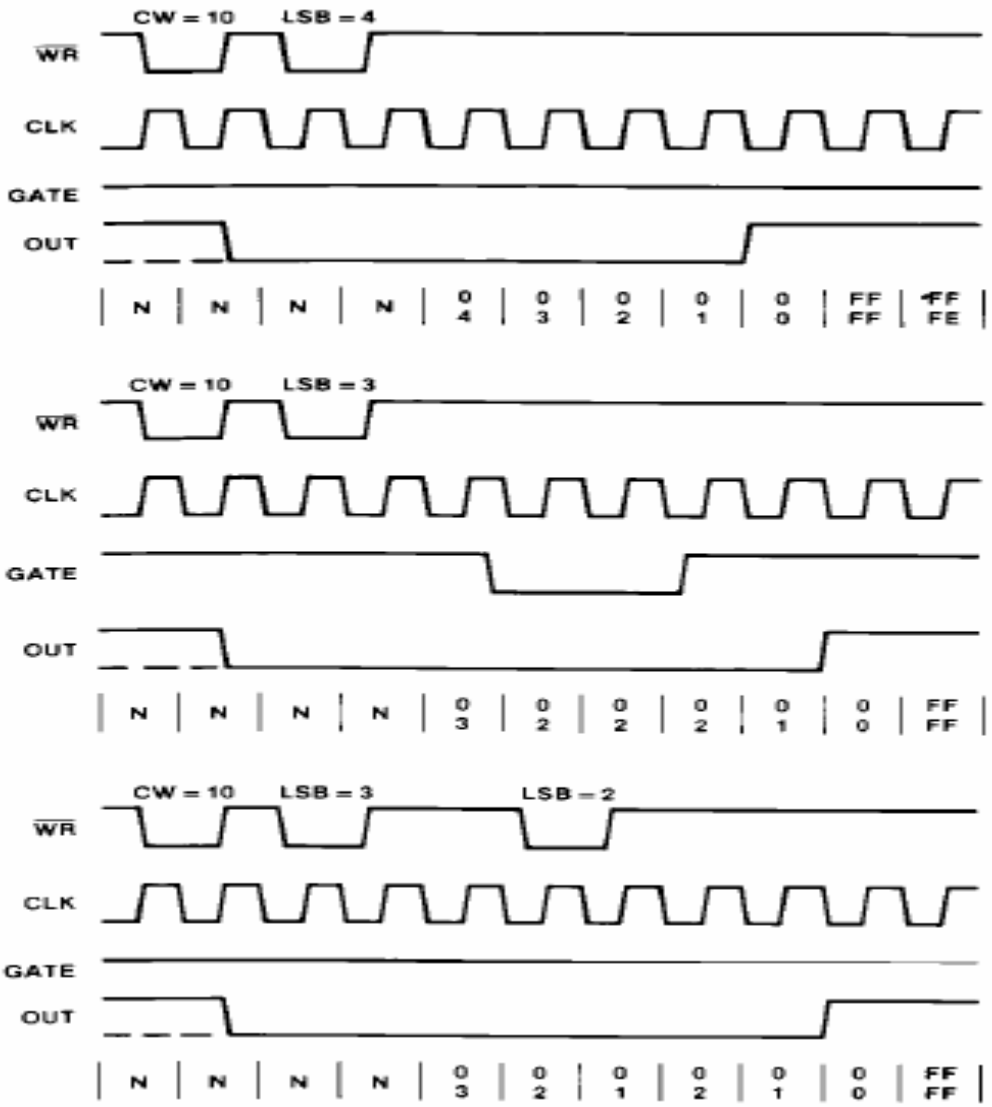
- Since the Control Word Register and the three Counters have separate addresses (selected by the A1, A0 inputs), and each Control Word specifies the Counter it applies to (SC0,SC1 bits), no special instruction sequence is required.
- Any programming sequence that follows the conventions is acceptable.
- A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.
- If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.
- **Read Operations**: It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 8254.
- There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command.
- Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic.
- Otherwise, the count may be in the process of changing when it is read, giving an undefined result.
-

Modes of Operation

MODE 0: **Interrupt on terminal count:**

- Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero.
- OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.
- GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.
- After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N a 1 CLK pulses after the initial count is written.
- If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
- Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
- Writing the second byte allows the new count to be loaded on the next CLK pulse.
- This allows the counting sequence to be synchronized by software. Again, OUT does not go high until Na1 CLK pulses after the new count of N is written.

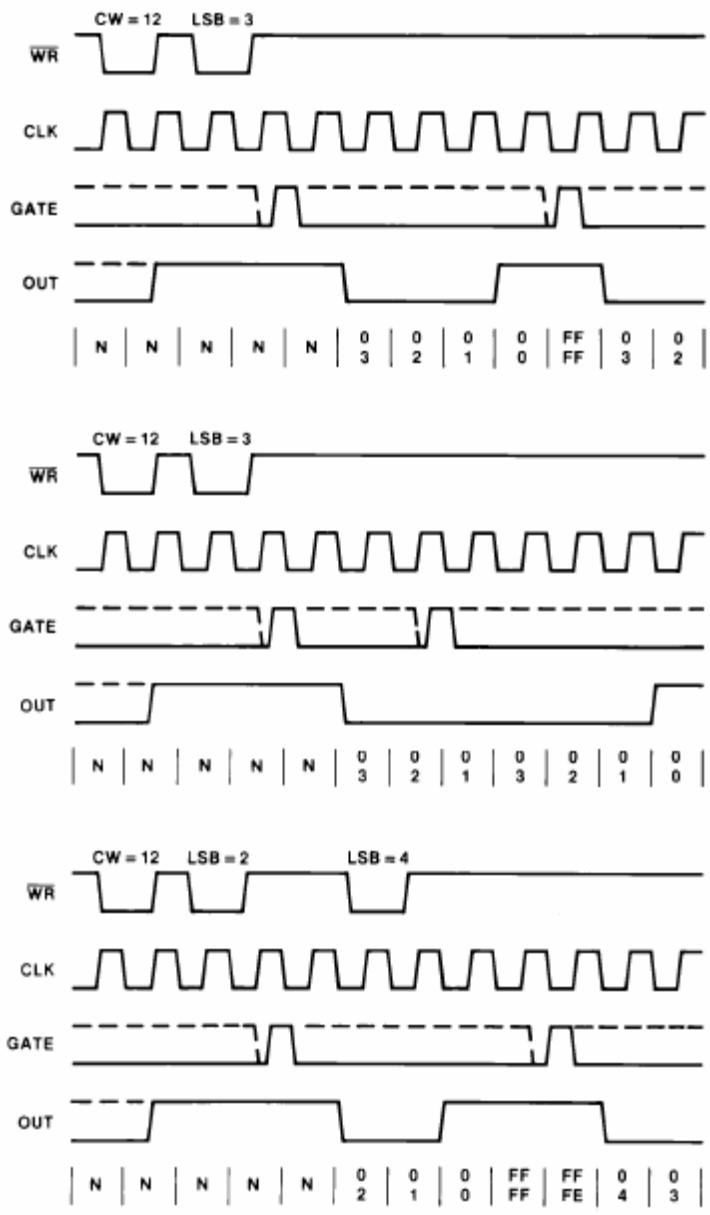
- If an initial count is written while GATE e 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.



MODE 1: Hardware retrigger able one-shot:

- OUT will be initially high.
- OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero.
- OUT will then go high and remain high until the CLK pulse after the next trigger.
- After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration.
- The one-shot is retriggerable; hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

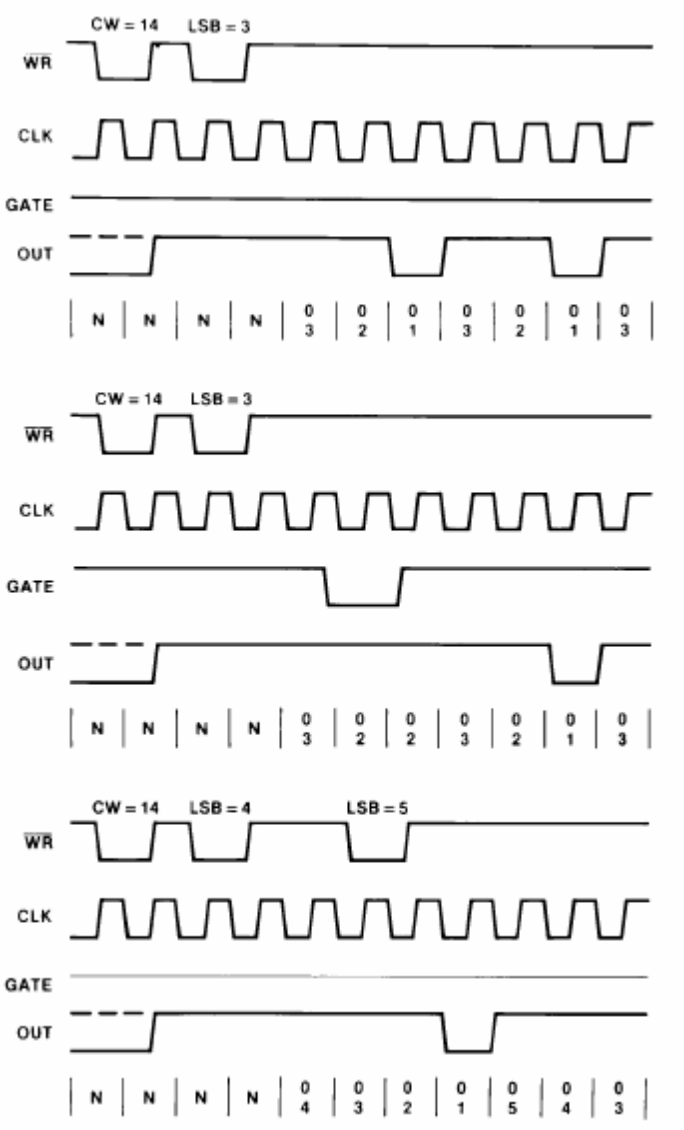
- If a new count is written to the Counter during a oneshot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the oneshot pulse continues until the new count expires.



MODE 2: Rate generator:

- This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt.
- OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated.
- Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.
- GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately.

- A trigger reloads the Counter with the initial count on the next CLK pulse, OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.
- After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written.
- This allows the Counter to be synchronized by software also. Writing a new count while counting does not affect the current counting sequence.

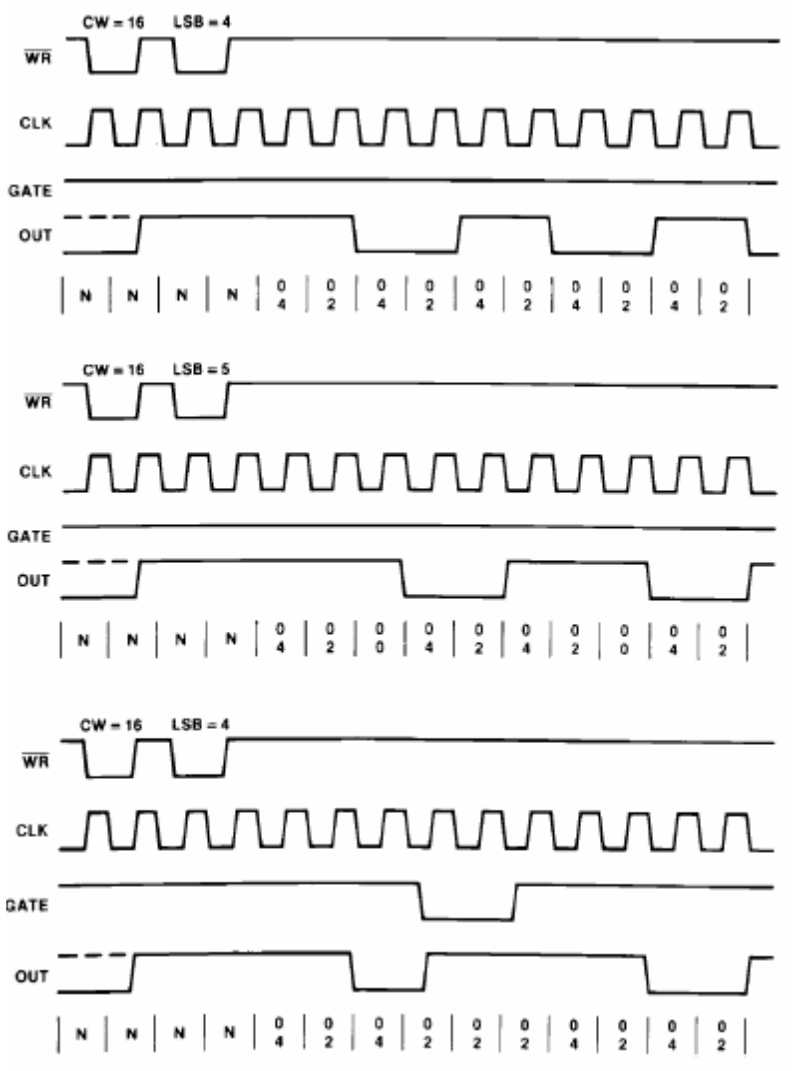


- When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely.
- An initial count of N results in a square wave with a period of N CLK cycles. GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required.
- A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.
- After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

- Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

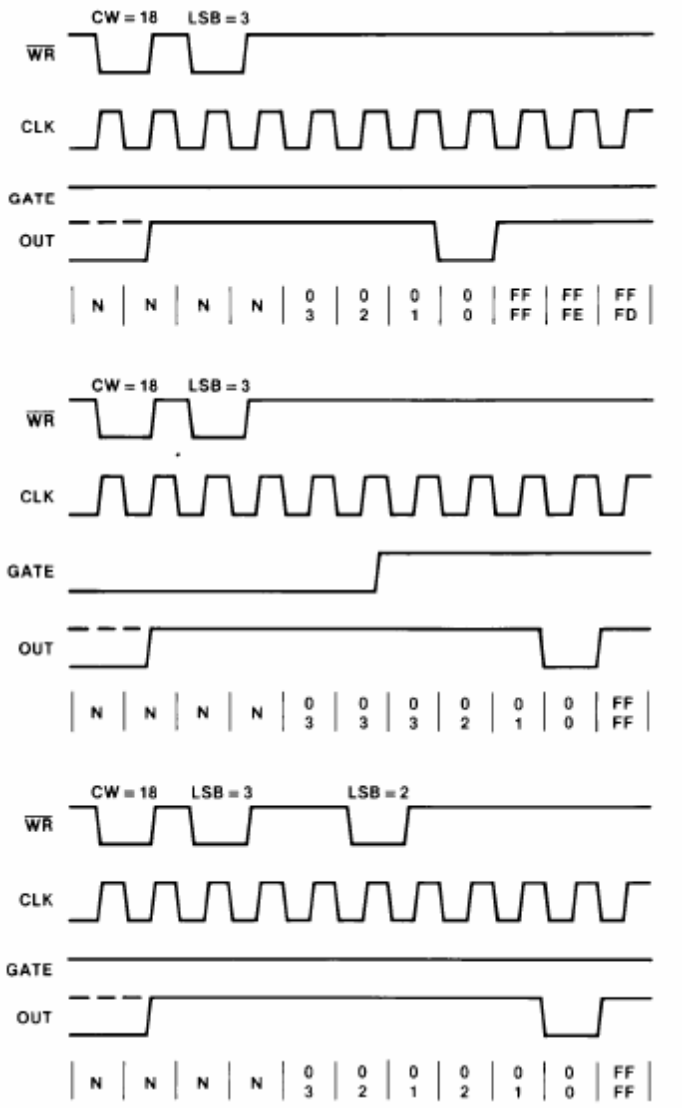
Mode-3 (Even Counter)

- OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses.
- When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.
- **Odd counts**: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses.
- One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one.
- Succeeding CLK pulses decrement the count by two.
- When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely.
- So for odd counts, OUT will be high for (N - 1)/2 counts and low for (N - 1)/2 counts.



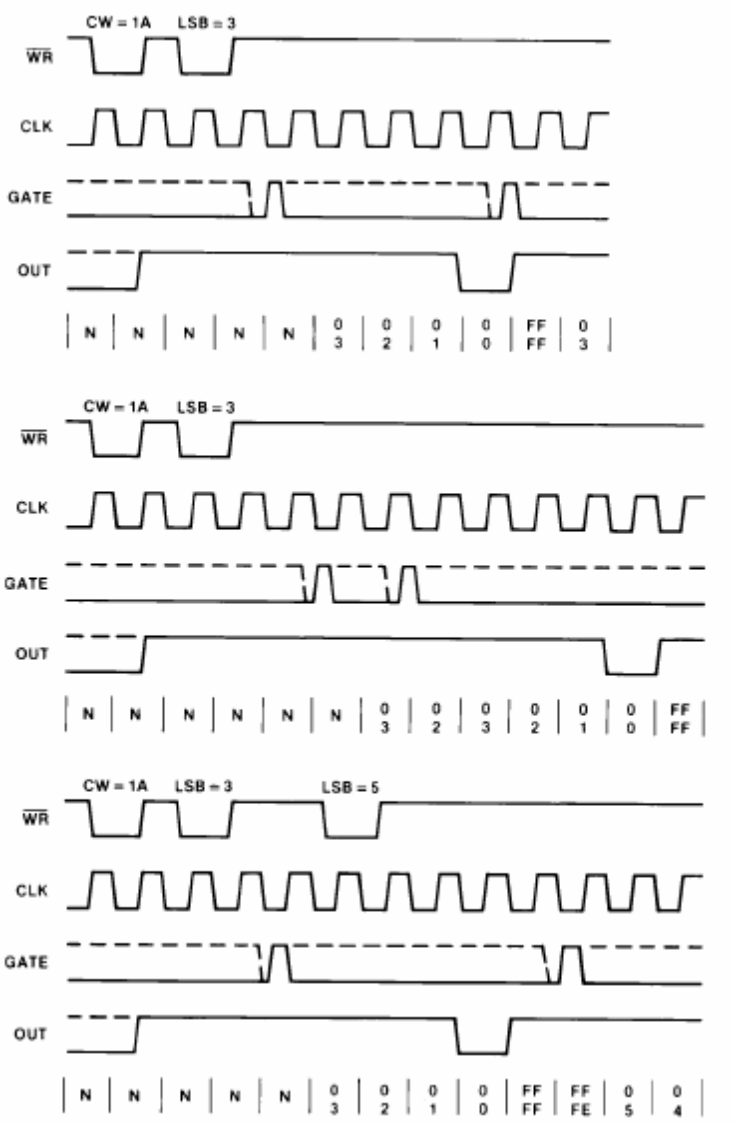
MODE 4: Software triggered strobe

- OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is ``triggered'' by writing the initial count.
- GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT. After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse.
- This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.
- If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
  1) Writing the first byte has no effect on counting.
  2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
- This allows the sequence to be ``retriggered" by software. OUT strobes low N a 1 CLK pulses after the new count of N is written.



MODE 5: Hardware triggered strobe (retriggerable):

- OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.
- After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N = 1 CLK pulses after a trigger.
- A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N a 1 CLK pulses after any trigger. GATE has no effect on OUT.
- If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.


CW = 1A
LSB = 3
WR
CLK
GATE
OUT
N N N N N 03 02 01 00 FFFF 03
CW = 1A
LSB = 3
WR
CLK
GATE
OUT
N N N N N N 03 02 03 02 01 00 FFFF
CW = 1A
LSB = 3
LSB = 5
WR
CLK
GATE
OUT
N N N N N 03 02 01 00 FFFF FFFE 05 04

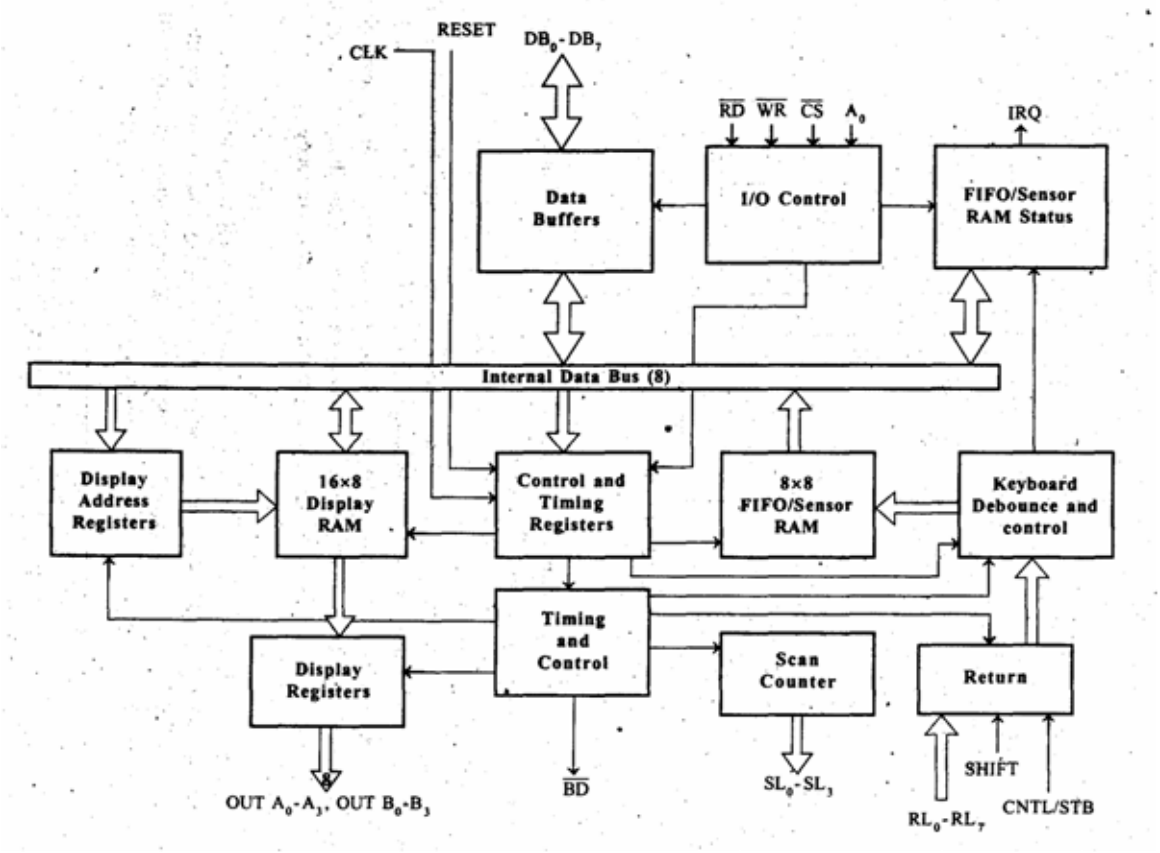
KEY BOARD/DISPLAY CONTROLLER - INTEL 8279

The INTEL 8279 is specially developed for interfacing keyboard and display devices to 8085/8086/8088 microprocessor based system. The important features of 8279 are,

- Simultaneous keyboard and display operations.
- Scanned keyboard mode.
- Scanned sensor mode.
- 8-character keyboard FIFO.
- 1 6-character display.
- Right or left entry 1 6-byte display RAM.
- Programmable scan timing.

Block diagram of 8279:

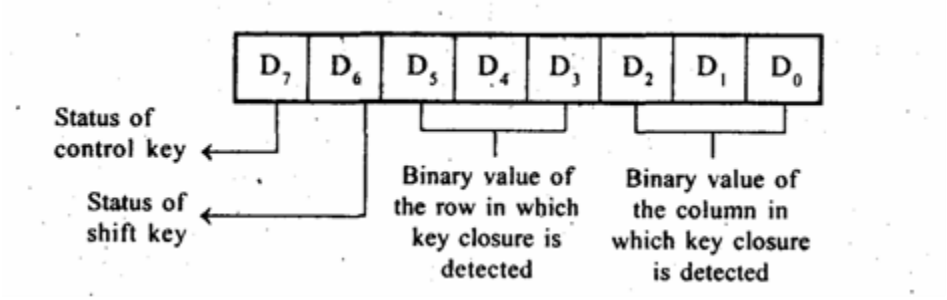
- The functional block diagram of 8279 is shown.
- The four major sections of 8279 are keyboard, scan, display and CPU interface.



Keyboard section:

- The keyboard section consists of eight return lines RL0 - RL7 that can be used to form the columns of a keyboard matrix.
- It has two additional input : shift and control/strobe. The keys are automatically debounced.

- The two operating modes of keyboard section are 2-key lockout and N-key rollover.
- In the 2-key lockout mode, if two keys are pressed simultaneously, only the first key is recognized.
- In the N-key rollover mode simultaneous keys are recognized and their codes are stored in FIFO.
- The keyboard section also have an 8 x 8 FIFO (First In First Out) RAM.
- The FIFO can store eight key codes in the scan keyboard mode. The status of the shift key and control key are also stored along with key code. The 8279 generate an interrupt signal when there is an entry in FIFO. The format of key code entry in FIFO for scan keyboard mode is,



- n sensor matrix mode the condition (i.e., open/close status) of 64 switches is stored in FIFO RAM. If the condition of any of the switches changes then the 8279 asserts IRQ as high to interrupt the processor.

Display section:

- The display section has eight output lines divided into two groups A0-A3 and B0-B3.
- The output lines can be used either as a single group of eight lines or as two groups of four lines, in conjunction with the scan lines for a multiplexed display.
- The output lines are connected to the anodes through driver transistor in case of common cathode 7-segment LEDs.
- The cathodes are connected to scan lines through driver transistors.
- The display can be blanked by BD (low) line.
- The display section consists of 16 x 8 display RAM. The CPU can read from or write into any location of the display RAM.

Scan section:

- The scan section has a scan counter and four scan lines, SL0 to SL3.
- In decoded scan mode, the output of scan lines will be similar to a 2-to-4 decoder.
- In encoded scan mode, the output of scan lines will be binary count, and so an external decoder should be used to convert the binary count to decoded output.
- The scan lines are common for keyboard and display.
- The scan lines are used to form the rows of a matrix keyboard and also connected to digit drivers of a multiplexed display, to turn ON/OFF.

CPU interface section:

- The CPU interface section takes care of data transfer between 8279 and the processor.

- This section has eight bidirectional data lines DB0 to DB7 for data transfer between 8279 and CPU.
- It requires two internal address A =0 for selecting data buffer and A = 1 for selecting control register of8279.
- The control signals WR (low), RD (low), CS (low) and A0 are used for read/write to 8279.
- It has an interrupt request line IRQ, for interrupt driven data transfer with processor.
- The 8279 require an internal clock frequency of 100 kHz. This can be obtained by dividing the input clock by an internal prescaler.
- The RESET signal sets the 8279 in 16-character display with two -key lockout keyboard modes.

Modes of Operation

In scanned keyboard mode with 2 key lockout, when a key is pressed, a debounce logic comes into operation. During the next two scans, the other keys are checked for closure and if no other is pressed the first pressed key is identified. The key code of the identified key is entered into the FIFO with SHIFT and CNTL status, provided that FIFO is not full, that is it has at least one byte free. If the FIFO does not have any free byte, naturally the key data will not be entered and the error flag is set. If the FIFO has at least one byte free, the above code is entered into it and the 8279 generates an interrupt (on IRQ line) to the CPU to inform about the previous key closures. If another key is found closed during the subsequent two sacns, no entry to FIFO is made. If all the other keys are released before the first key, the key code is entered into FIFO. If the first pressed key is released before the others, the first will be ignored. A key code is entered to FIFO only once for each valid depression, independent of other keys pressed along with it, or released before it. If two keys are pressed within a debounce cycle (simultaneously) no key is recognized till one of them remains closed, and the other is released. The last key that remains depressed is considered as single valid key depression.

In scanned keyboard with N-key rollover each key depression is treated independently. When a key is pressed the debounce circuit waits for two keyboard scans and then checks whether the key is still depressed. If it is still depressed, the code is entered in FIFO RAM. Any number of keys can be pressed simultaneously and recognized in the order, the keyboard scan recorded them. All the codes of such keys are entered into FIFO. Note that, in this mode, the first pressed key need not be released before the second is pressed. All the keys are sensed in the order of their depression, rather in the order the keyboard scan senses them, and independent of the order of their release.

The scanned keyboard special error mode is valid only under the N-key rollover mode. This mode is programmed using end interrupt/error mode set command. If during a single debounce period (two keyboard scans) two keys are found pressed, this is considered a simultaneous depression and an error flag is set. This flag, if set, prevents for the writing in FIFO, but allows generation of further interrupts to the CPU for FIFO read. The error flag can be read by reading the FIFO status word. The error flag is set by sending normal clear command with CF = 1.

In the sensor matrix mode, the debounce logic is inherited. The 8-byte FIFO RAM now acts as 8*8 bit memory matrix. The status of the sensor switch matrix is fed directly to sensor RAM matrix. Thus the sensor RAM bits contain the row wise and column wise status of the sensors in the sensor matrix. The IRQ line goes high, if any change in sensor

value is detected at the end of a sensor matrix scan or the sensor RAM has a preivous entry to be read by the CPU. The IRQ line is reset by the first data read option, if AI = 0, otherwise, by issuing the end interrupt command. AI is a bit in read sensor RAM word.

There are various options of data display. For example, the command number of characters can be 8 or 16, with each character organized as single 8-bit or dual 4-bit codes. Similarly, there are two display formats. The first one is known as left entry mode or type writer mode, since in a type writer the first character typed appears at the left most position, while the subsequent characters appear successively to the right of the first one. The other display format is known as the right entry mode, or calculator mode, since in a calculator the first character entered appears at the rightmost position and this character is shifted one position left when the next character is entered. Thus all the previously entered characters are shifted left by one position when a new character is entered.

In the left entry mode, the data is entered from the left side of the display unit. Address 0 of the display RAM contains the leftmost display character and address 15 of the RAM contains the right most display character. It is just like writing in our note books, i.e., from left to right. If the 8279 is in auto increment mode, the display on the leftmost display and the sixteenth entry on the rightmost display. The seventeenth entry is again displayed at the leftmost display position.

In the right entry mode, the first entry to be displayed is entered on the rightmost display. The next entry is also placed in the right most display but after the previous display is shifted left by one display position. The leftmost character is shifted out of that display at the seventeenth entry and is lost; it is pushed out of the display RAM.

Interfacing 8279 with 8085 processor:

- A typical Hexa keyboard and 7-segment LED display interfacing circuit using 8279 is shown.

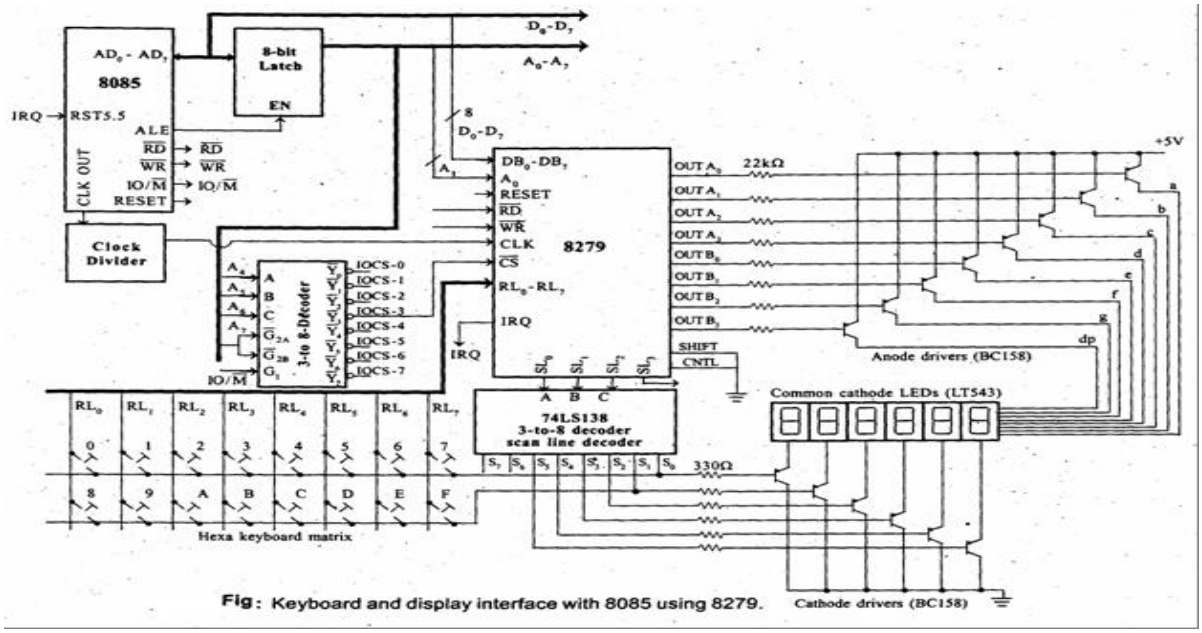


Fig: Keyboard and display interface with 8085 using 8279.

Serial Data Transfer

The microprocessor is a paroled device it transfers eight bits of data simultaneously over eight data lines. This is pirated S/o mode.

- Pirated data communication over a long distance an become very expensive. Exa – CRT terminals or cassette tapes.
- But on serial I/o mode, one be/- at a time is transferred over a single lines.
- In serial transmission, an 8-bit parallel ward should be converted into a stream of 8 serial bits, this is known as pirated to serial conversion. After conversion one bit at a time is transmitted over a single line of a given rate called the based (bits per second).
- In serial reception, the MPU receives a stream of eight bits and they should be converted into an 8-bit parallel word, this is known as serial to parallel conversion.

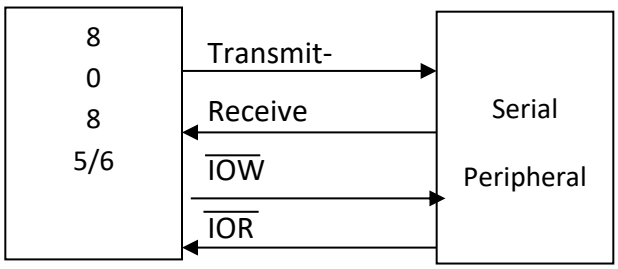
Basic Concepts in Serial I/O

Interfacing requirement: The interaction requirements for a serial I/O peripheral are the sane as for a parallel I/O device.

The UP identifies the peripheral through a part address and enables it using the read & white control signals.

The primary difference bet. Serial and parallel data transfer

1. The parallel I/O uses the entire data bas and the serial I/O uses one data line.
2. Parallel data transmission is expensive than the serial.
3. Serial data transmission is used for long distance block diagram for serial I/O interfacing.



As a typical configuration of serial I/O transmission. MPU selects the peripheral through chest select and the control signals read (WR) to transmit data. The address decoding be other peripheral can be interfaced under either program control (stats check) or intercept control.

FORMAT- In the synchronies formula a receiver & a transmitter are synchronized. A block of characters is transmitted along with the synchronization information.

It is generally used for high speed transmission (more than 20Kbs).

Fig

In the asynchronous formula each character curries the information it the start a the stop bits. When no data are being transmitted, a receiver stays high at logic 1, welled Mark logic O is could space-

- The transmission begins with one start bit (low), followed by a character and one stop bits (high). This is also know as framing.
- Asynchronous formula is used in low sped transmission.

  Fig:

  Transmission
- In serial I/O, one bet- is seat out at a time therefore how long the bit stays on or different is determined by the speed at which the bits are transmitted.
- The receiver should be up to receive the bite at the same rate as the transmission, otherwise the receiver may not be able to differentiate bet. Two consecutives 0'6 or 1'5.
- The rate at which the bits are transmitted is called bits per second or bared.

Fig:

Fcy shoes who the ASCII character 'I' (49H) will be transmitted with 1200 bared with the framing information if one start a two stop bits. The transmission begins with an active low start bit, followed by LSBCDO)

1200 bits = 1 second

1 bit $= \frac{1}{1200}$ = 0.83ms

Error checks in Data Communication

- Parity check

- Checksum
- Cycler Redundancy check (CRC)

Data Communication over Telephone Lines

Generally the telephone lines are designed to handle voice of band width ranges from 300Hz to 3300 Hz.

A modem (Modulator/demodulator) is a device that translates digital data into audio tone frequencies for transmission over telephone lines and converts audio frequencies into digital dat for reception.

Generally two types of modulator scheme are used.

i) Frequency shift keying (FSK) for low speed modem.

ii) Those shift keying (FSK) for high speed modem.

USART (Intel 8251)

This chip is called universal synchronous asynchronous receiver transmitter. This is exclusively used in senile data transfer.

Serial data transfer:- The 8085 is a parallel device, it transfer 8-bits of data simultaneously over 8 data lines. This is called parallel 9b mode.

- Parallel data communication over a long distance can become very expensive.
- But in serial 9/o mode, one bit at a time is transferred over single lines.
- So in serial transmission, as 8 bit parallel word shield be converted into strum it eight servile bots known as paneled to senoel conversion.
- After taken conversion one bit at a time is transmuted over a single time at a gives rate called baud rate.
- In serial reception the MHU receives a stream of 8-bits & they should be converted into 8-bit parallel word could serial topical serial conversion.

Format for serial communication

- Synchronies format
- Asynchronous format

In synchronous format, a receiver & a transmitter are synchronized, a block of characters is transmitted along with synchronic information. It is

generally used for high – speed transmission. In asynchronies format each character carries the information of the start & stop bots.

- When no data is transmitted, a receiver stays high at logic 1 called mark at logic o is called space.
- The transmission begins with one start bit (100) followed by character & one or more stop bits (high). This is known as framing.
- It is used in low speed transmission.

  USART is a programmable device which is used for serviced data communication. It has the following section.

  i) Read / Wile control logic.

  ii) Transmitter.

  iii) Recover.

  iv) Data bus buffer.

  v) Modem control.

Fig:

Control logic:-This logic interfaces the chip with the MPU, determines the determines the factions of the chief according to the control word in the register and monitors the data flow.

FX section: This converts the parallel word recovered from the MPU into several bits & transmits them over the TxD line to a peripheral.

Rx Section: This section receives serial bits form a peripheral, convents them into a parallel word & transfer the word to the MPU.

Modem Control: The modem control is used to established data common through modem over telephone line.

ARCHITECTLRE OF 8251

Read / Write Control logic & Registers

This section includes R/W control logic sit i/p signals, control logic & 3 buffer registers, line data register, control register status register. The regales associated with these over follows:-

Is (chip select):-When this signal goes low the 8251 is selected by 8251 MDU for communication. This is usually contacted to a decoded address bus.

Fig: Block of control logic & Register)

C/D = 1⟶ Control or statues register is selected

0 ⟶ Data butter is selected.

The control & status register are differentiated by WE & RD signals respectively by WR & WD signals respectively

WR⟶ 0⟶ MPU either writes in control register or send output to data buffer. This is connected to IOW or MENW.

RD⟶ 0⟶ MPS either reads a status from.

Status register or accepts data form data buffer. This is connected to 90R or MEMR

Reset

A high on this input resets the 8251A & forces it into the idle mode.

CLK (Clack) This is he clock input usually connected to the system clock. This clock does not control either the transmission or reception rate matter it is necessary for communication with

Control Register:- This is a 16-bit register for a control word consists of 2 independent byte . The 1st bite is called mode instruction word & 2nd byte is called command instruction (word). This register can be accessed as on o/p purl when C/D is high.

Status Register: This i/p register checks the ready status of a peripheral. This register is addressed as an e/p port when C/D is high. It has the came port address as the control register.

Data Bitter: This is a bi-direct control register can be addressed as an i/p port & an o/p port when c/d pin is low.

CONTROL WORD: The control cords are divided in too formats:- mode word and command word. The mode word specifics the general characters picas of operation (such as baud, parity on if of bits) whereas command word enables the data transmission & receptions.

Model Word Format

Fig:

WAP to enable USART to transmit serial data who 8251 operating in asynchronies model based rate 1200. The character length is 8-bits and the no of step bits is 2. Odd parity is used clock rate is 76.8kttz.

Status Register : It is used to indicate the status of transmitter & receiver sections. The do bit is used for transmitter ready signet. It is 1, it indicates the transmitter is empty and it can accept he data from up. D_1 bit is used to indicate the receiver ready signal. If it is 1, indicates that there is a data is the receiver butter register and the up has to read this data. If D_2 = 1, it indicates that the output butter register in the transmitter section is empty.

Specify the interdiction for the following parameter.

- With baud 9600
- Character length = seven bits with two stop bits
- No parity check
- T_x clock feq = 153.6 kHz

Write an instruction sequence to load control word FF into memory mapped 8251A with control register low located at address MODE what are the character length, type of parity and no of stop bits.

This section accepts parallel data from MPU & converts then into serial data. It has registers (i) Butter register to hold 8-bits (ii) O/P register to convert 8-bits into a stream of serial bits.

There O/P signal & one E/P signal are associated with this section.

T_xD (Transmit Data)- Serial data are transmitter on this pin.

T_xC (Transmitter Clock):- Controls the speed of transmission (rate at which bite are transmitted by USART). The clock frequency an be 1, 16, 64 times backed.

TxRPY (Transmitter Ready):- This is an D/P signal, when it is high. It indicates that he butter register is empty a the USART is needy to accept a byte. It can be used either to interrupt the MPU or to indicate the status. This signal is reset when a data byte is loaded into the butter.

T_xE (Transmitter comply):- This is an O/P signals A high signal in this line indicates that the O/P register is empty. This signal is reset when a byte is transferred from the butter to the O/P register.

The receiver accepts serial data on the R_xD line from a penihercel & converts them into parallel data.

i) Receiver e/p register

ii) Bitter register

The following place are associated:-

R_xD (Received data):- Bits are received serially on this time & converted into parallel byte in the receive i/p register.

R_xC (Receiver clock):- This is a clock *****control the received data rale.

P_xRDY (receiver Ready):- This is an o/p signal. It goes high when USART has a character in the buyer register & is ** it to MPU. This tine are be used either to indicate status or to *** MPU.

INITIALIZING THE 8251- In communicate through MPU 8251, the MPU must convery be 8251 modem bu**********

RS2325:-It is a 25 pin connector. It is used to imperfect a MODEM with a minicomputer through 8251A. It is a serial communication standard. inRs.2320, -12V is used to represent logic 1 & +12V for logic 0. It is a voltage fended for transmitting serial bits. This is acted negative true legit.